

MS-7676 Ver: 4.0 m-ATX : 245 X 245mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(Z68/H67)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 2

PCI Express (X1) Slot * 2

PWM:

Controller:VRD12 Ut501 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: UP6103 A

CPU SA : OP+MOS

DDR: UP6103A

PCH: UP6103A

ACPI:

UPI

Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x6

USB3.0 RearX2

D-SUB/DVI/HDMI *1

TPM Header *1(debug only)

on BOARD BUZZER

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三個BOM:

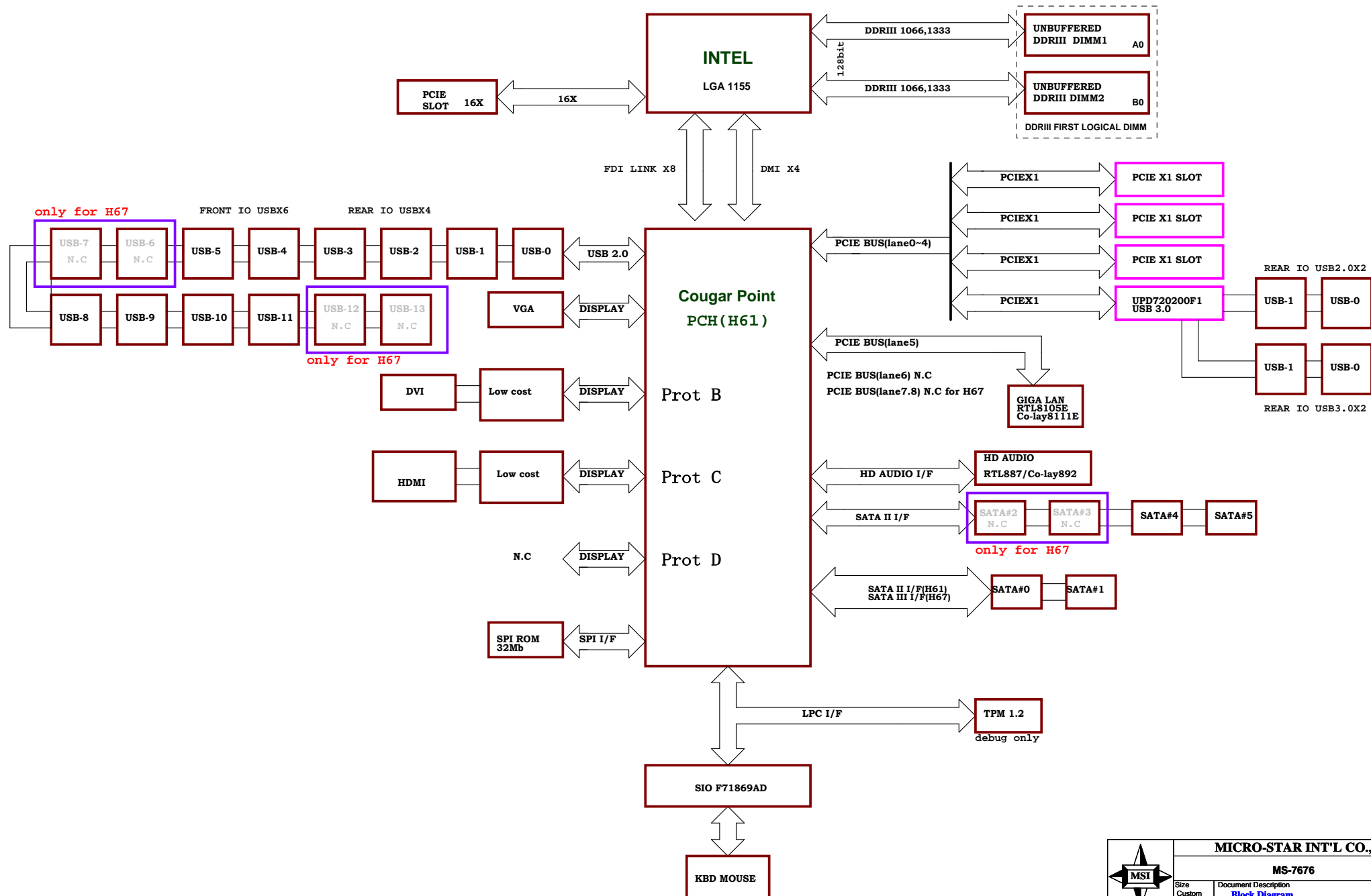
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- 2.H61 Full Spec(全固)
- 3.H61 common Spec(半固)



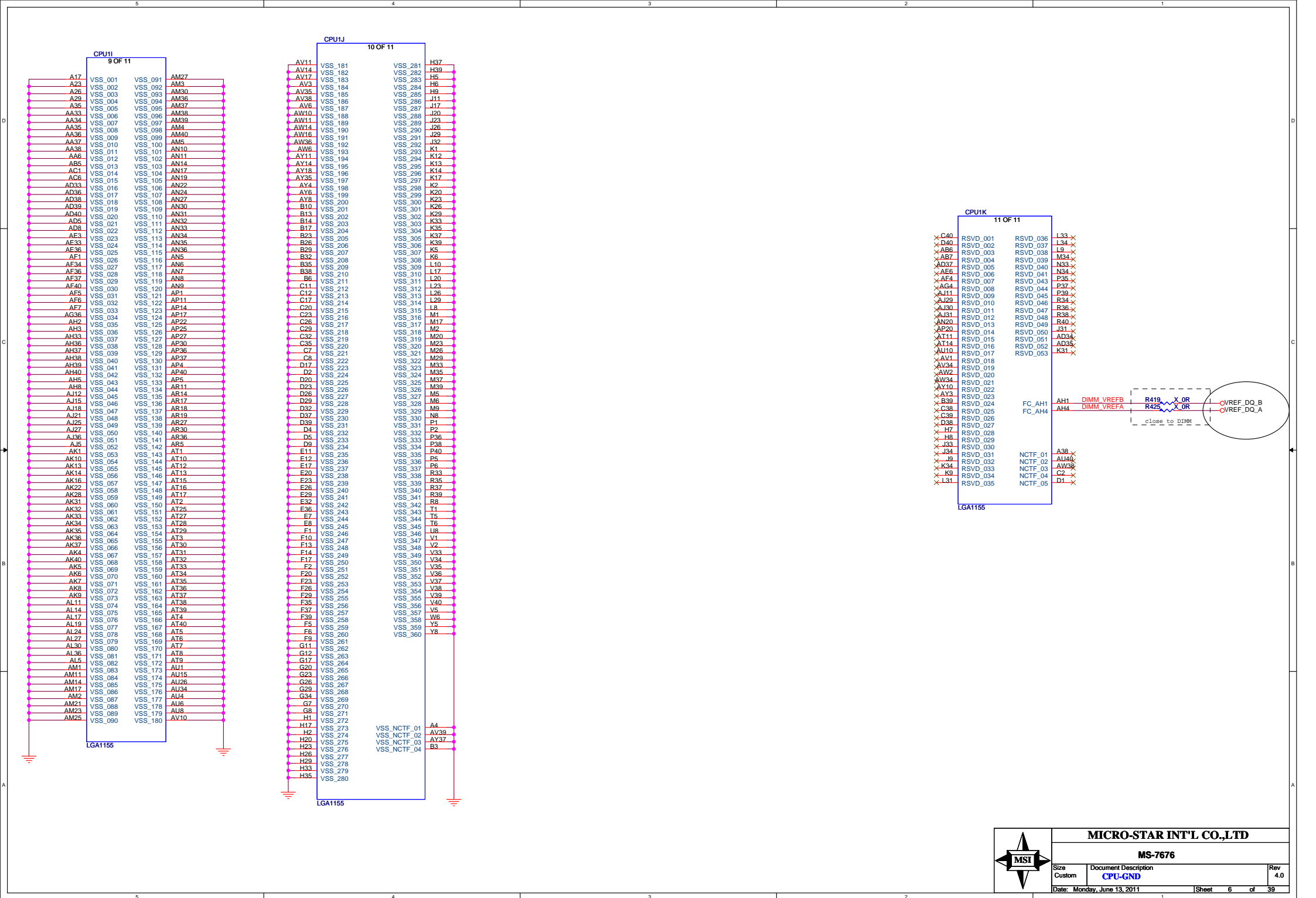
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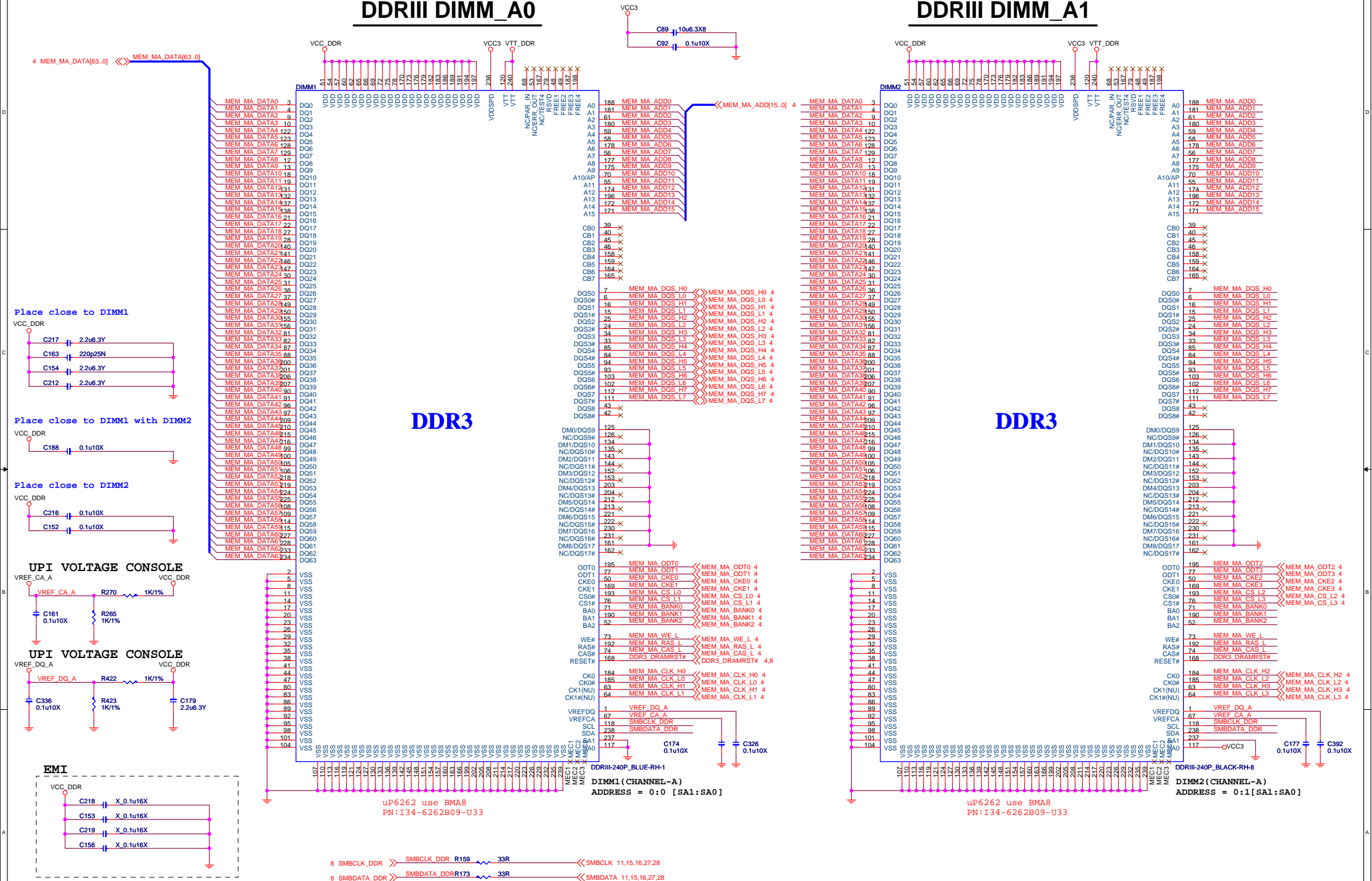




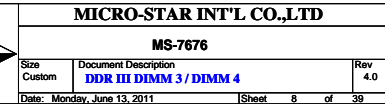


DDRIII DIMM_A0

DDRIII DIMM_A1



DDRIII DIMM_B1



REQUIRED STRAPS

Internal pull-up
Internal pull-up

FP_RST# R564 X 10K/1%
SIO_PME# R703 10K/1%
SPL_HOLD_GPO# R641 X 0.2K
PCIECLKREQ2# R575 X 10K/1%
PCIECLKREQ5# R642 X 10K/1%
PCIECLKREQ6# R547 X 10K/1%
PCIECLKREQ7# R645 X 10K/1%
SPL_LANE# R647 X 10K/1%
PCH_GPIO24 R655 X 220R
PCH_GPIO28 R623 X 10K/1%
PCH_GPIO72 R538 10K/1%
SB_WAKE# R636 1K
Ri# R658 10K/1%
SMLINKO_CLK R668 10K/1%
SMLINKO_DATA R669 10K/1%
PCH_SMLALERT# R660 10K/1%
PCH_SML1CLK# R659 10K/1%
PCH_SML1DATA R674 10K/1%
PCH_SML1ALERT# R697 10K/1%

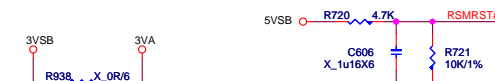
CRS pull down
PCH_GPIO57 R690 10K/1%
R669 X 10K/1%

SUSWARN#_CP R682 X 0R
RSMRST# R606 X 0R

PCH_GPIO31 R675 10K/1%
PCH_GPIO27 R762 10K/1%
SUSACK#_CP R16 10K
DPWROK_CP R25 10K

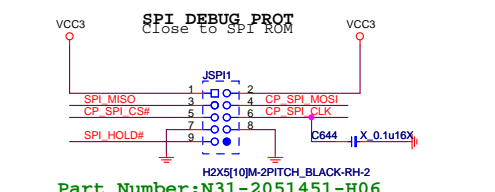
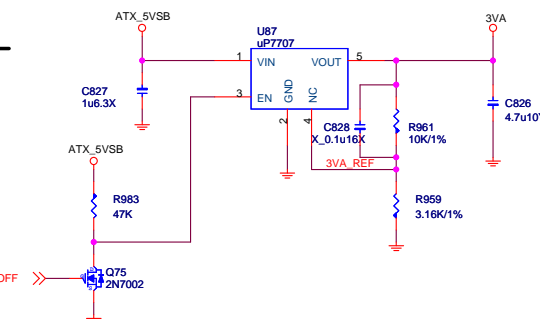
PCIECLKREQ2# R574 10K/1%
PCIECLKREQ5# R634 10K/1%
PCIECLKREQ6# R539 10K/1%
PCIECLKREQ7# R640 10K/1%
PCH_GPIO33 R717 X 1K

PCIECLKREQ can't find 0/1/3/4



3VA

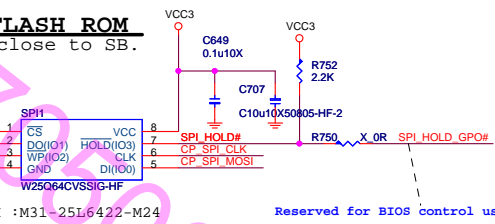
20mA



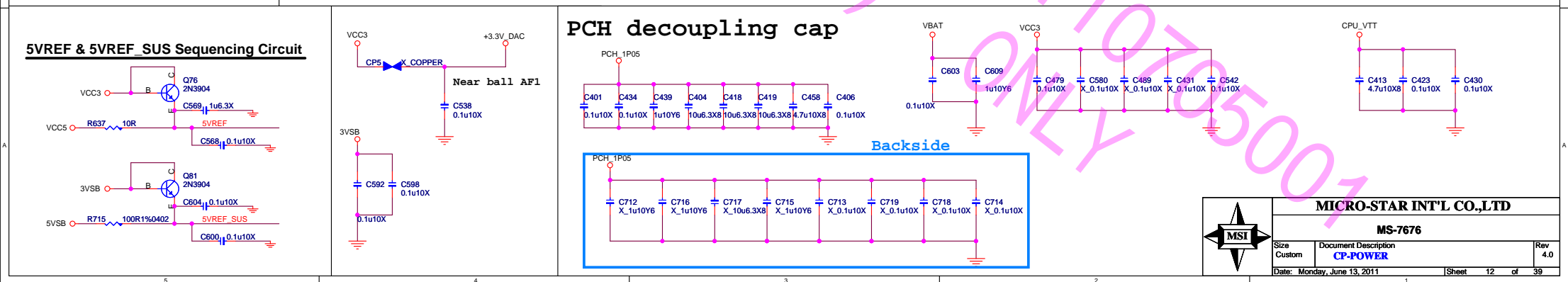
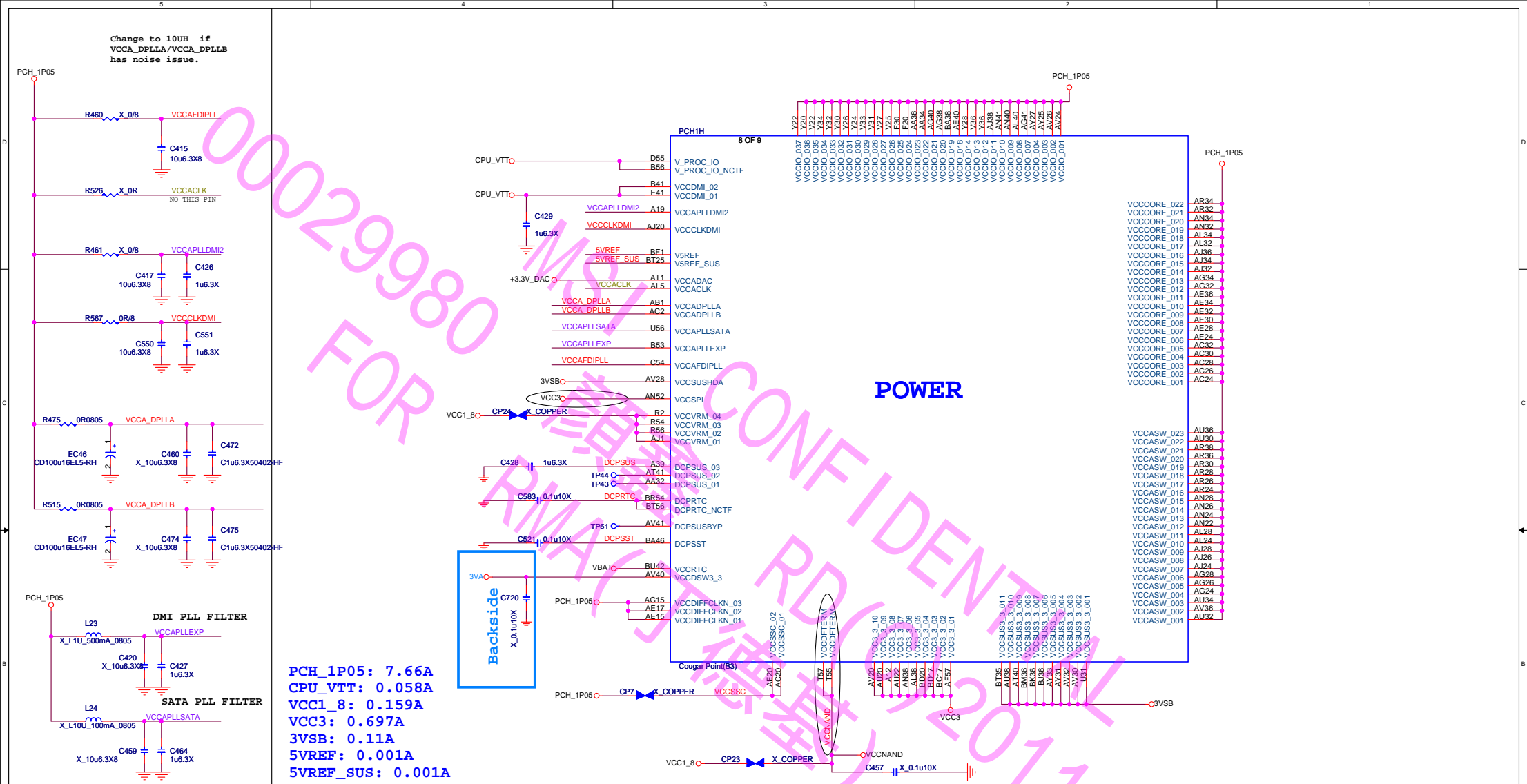
Part Number: N31-2051451-H06

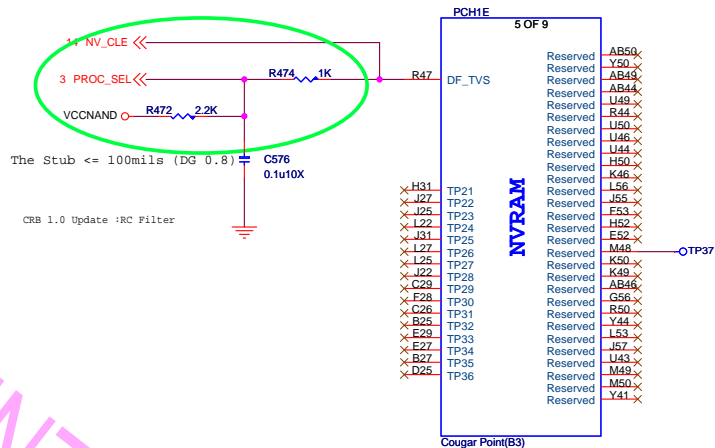
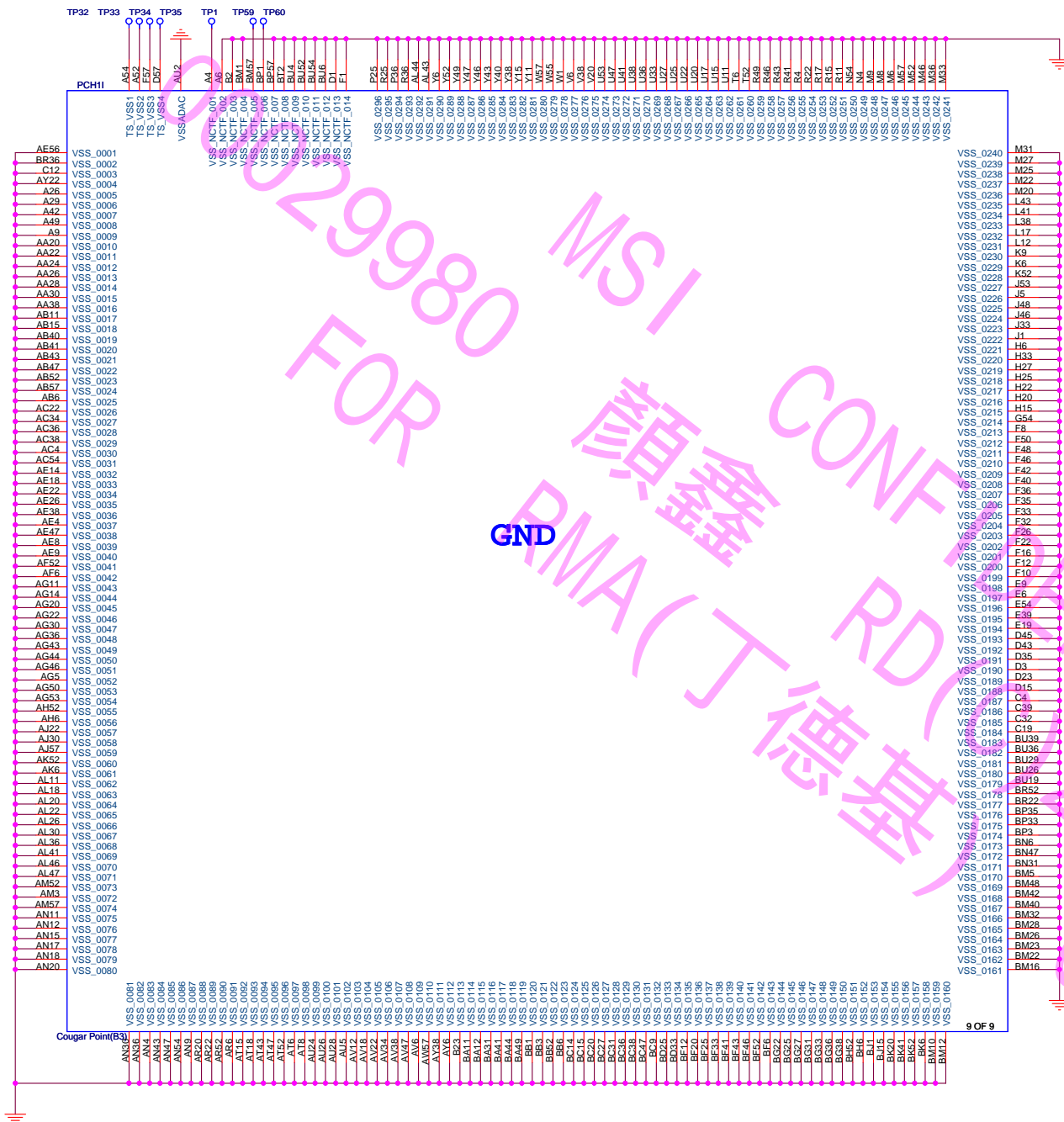
SPI FLASH ROM

Place close to SB.



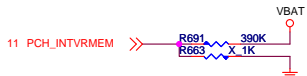
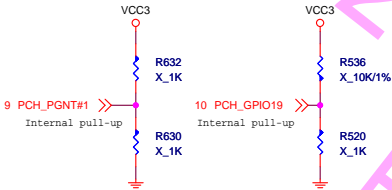
MICRO-STAR INT'L CO.,LTD			
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PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



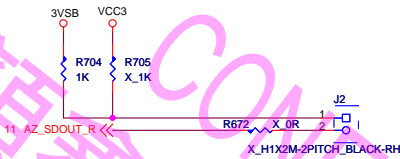
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



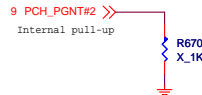
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be reconnected even when not supporting DSW.

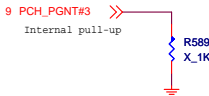


HDA_SDO
Disable ME in Manufacturing Mode when pull LOW ????

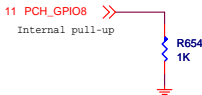
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high



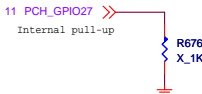
DMI AC/DC MODE
0 : AC
1 : DC *



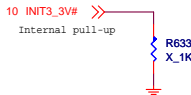
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

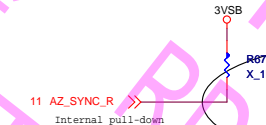


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INIT3_3V#
0 : ??????????????
1 : ?????????????? *

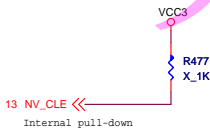
1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.



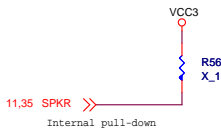
HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

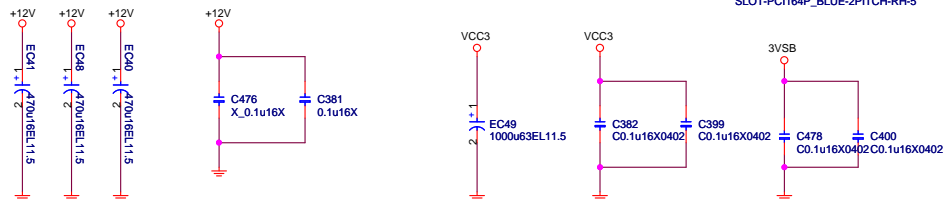
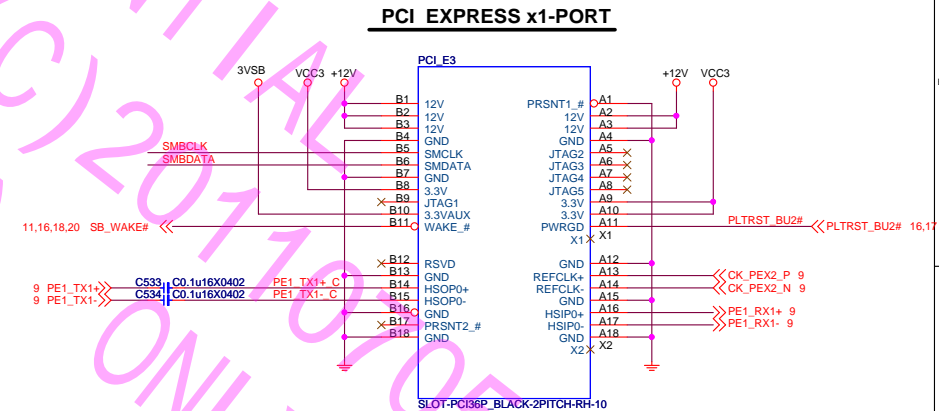
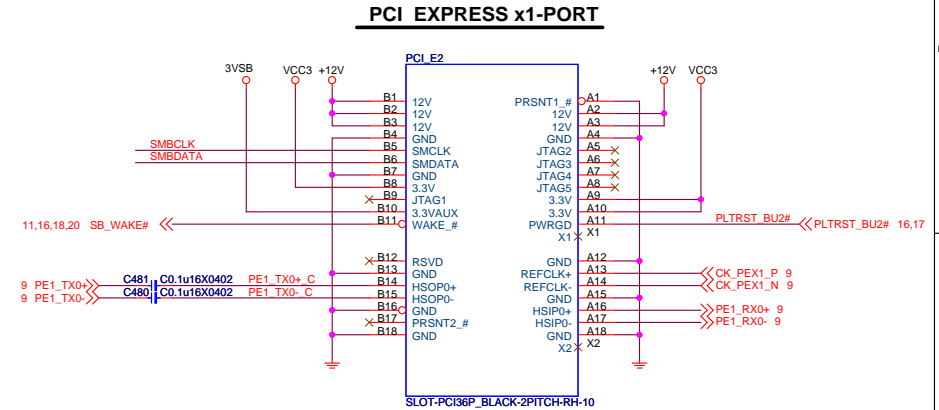


SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



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PCI_Express X16 Slot

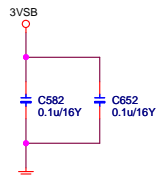
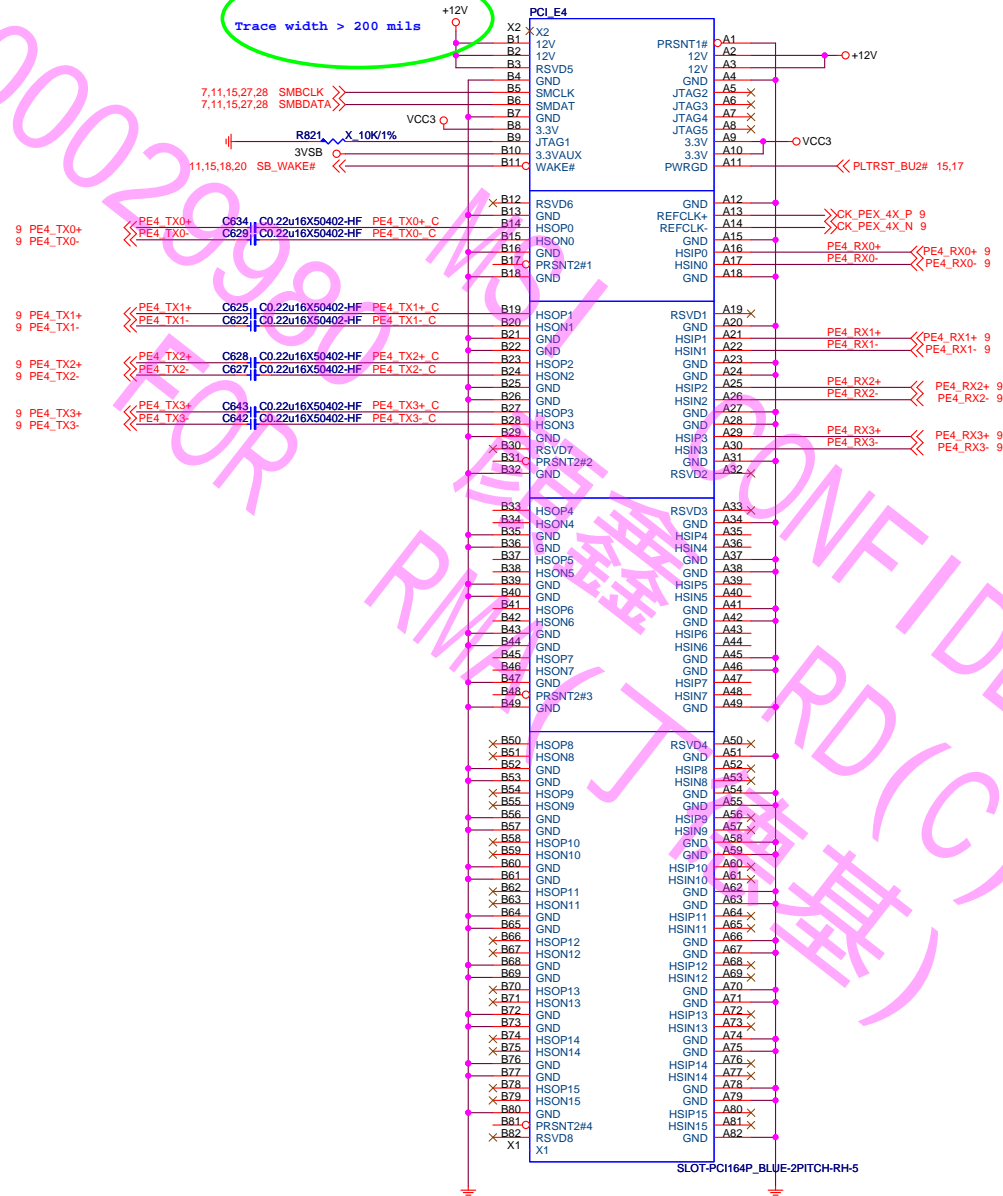


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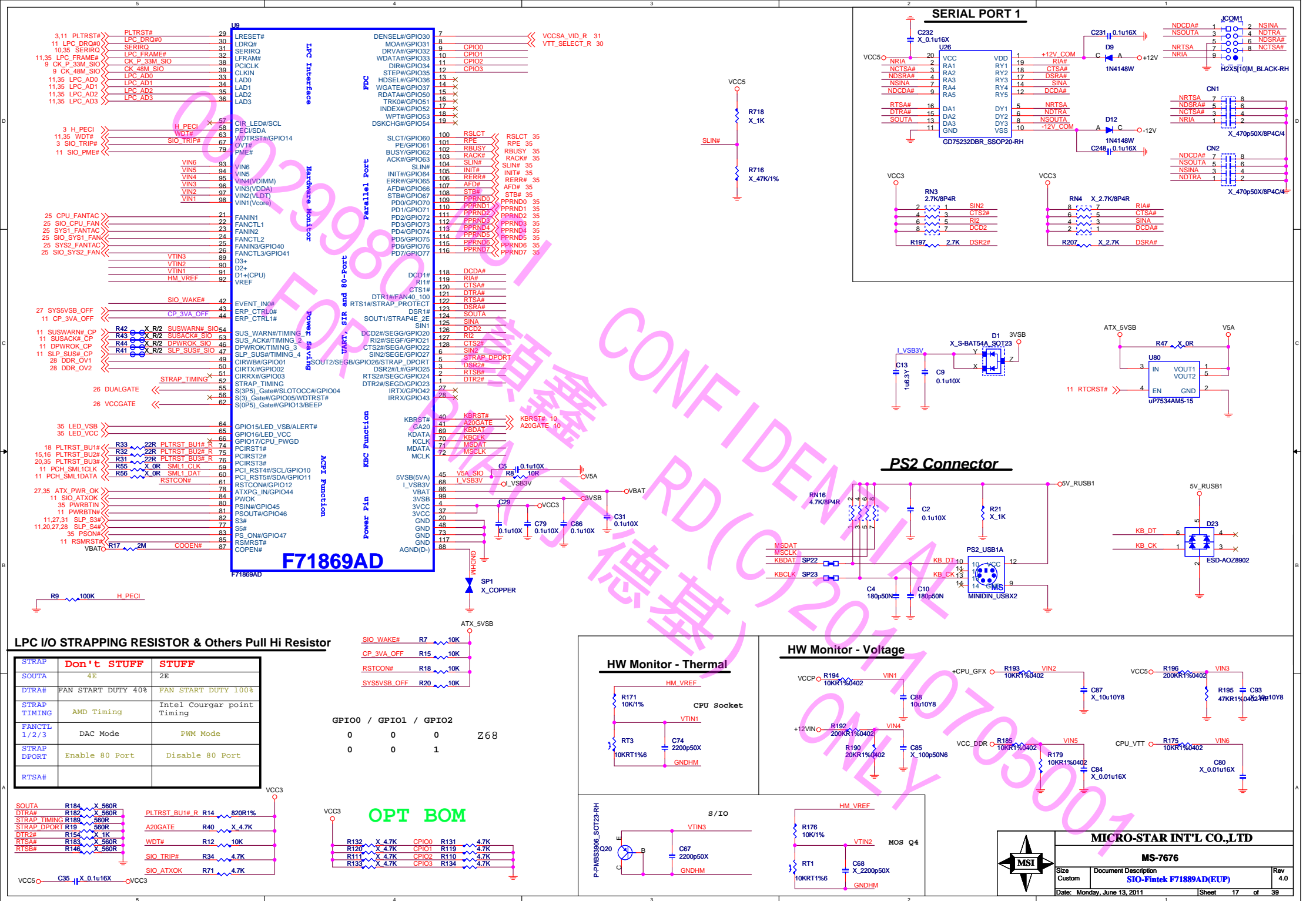
PCI_Express X4 Slot



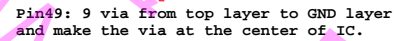
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RTL8105E 10/100M LAN



Place near pin

3VSB

CP14 X COPPER

CP6 X COPPER

VDD33

27 39 42 47 48 12

C436 X0/n1,0

C409 X0/n1,0

C407 X0/n1,0

C411 X0/n1,0

C410 X0/n1,0

C438 X0/n1,0

811E: stuff

8105E: unstuff

Place near pin

VDD10

3 13 19 45 41 6 9

C416 0.1u10X

C446 0.1u10X

C433 0.1u10X

C412 0.1u10X

C408 0.1u10X

C424 0.1u10X

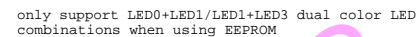
C435 0.1u10X



R Consumption

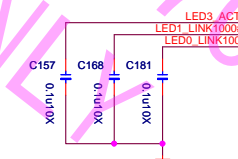
	3.3V	mW
811E: stuff		
8105E: unstuff		

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

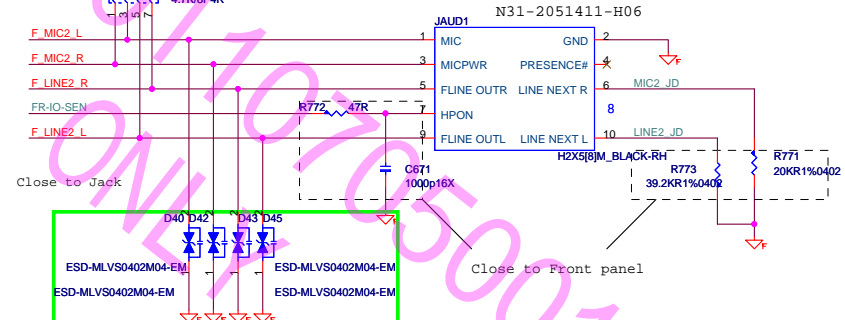
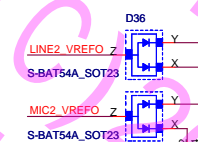
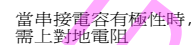
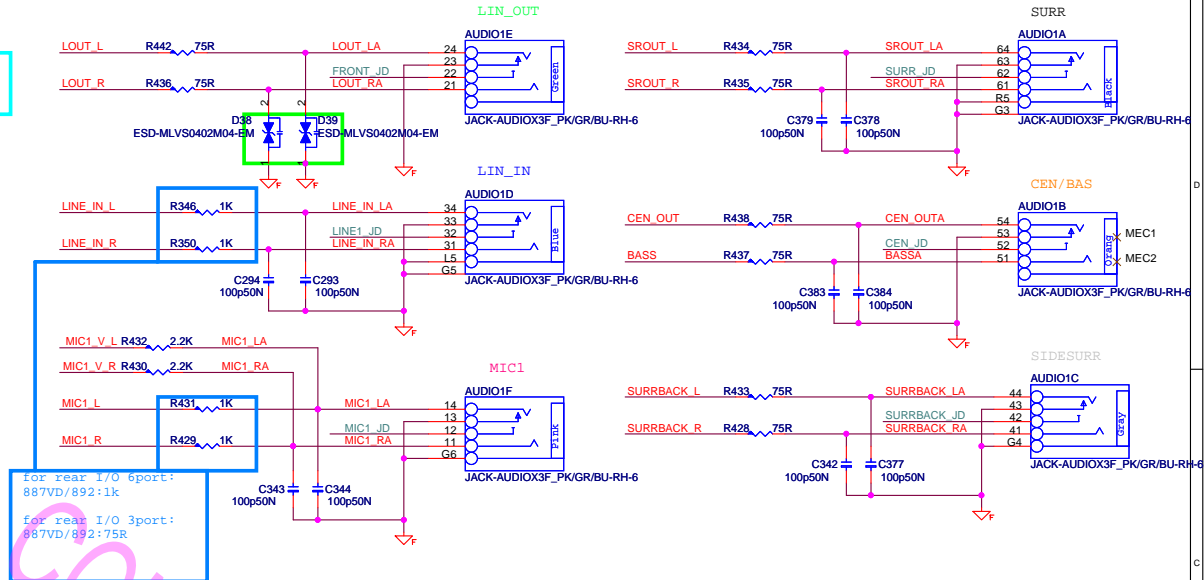
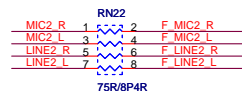
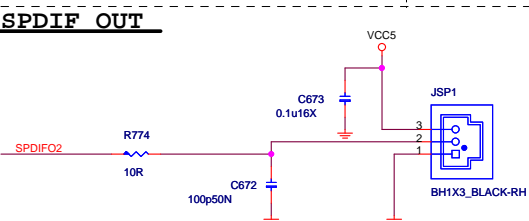
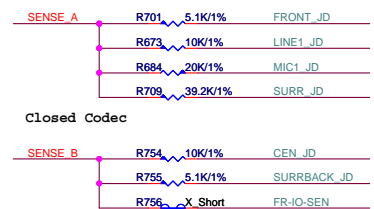
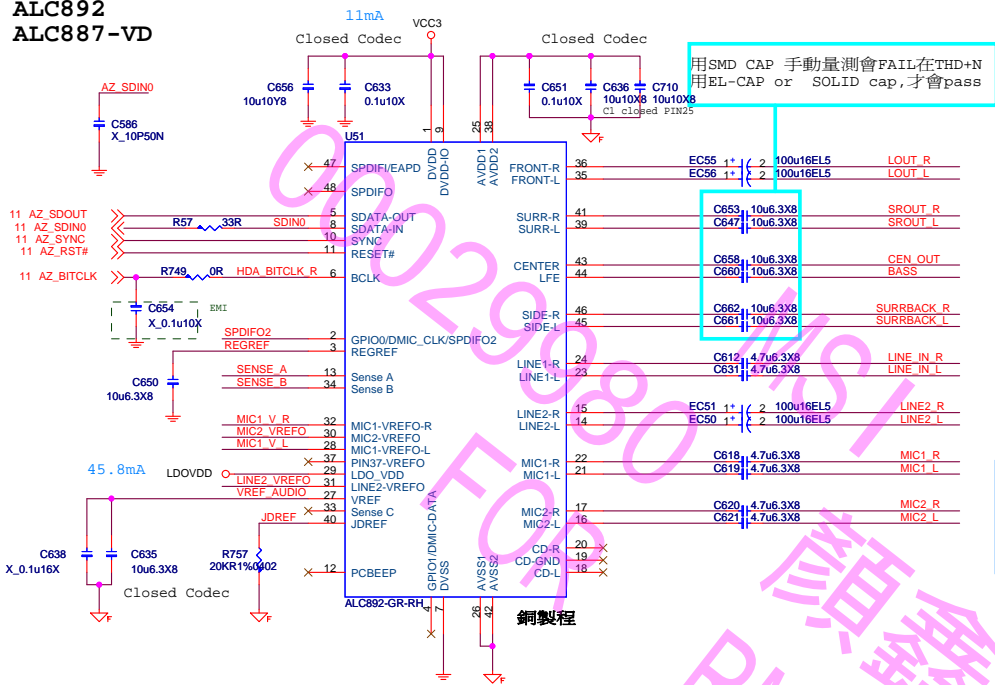


Giga-Lan		10/100-Lan	
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None		N58-22F0771 Link Yellow Active Blinking 100 Green 10 None	
19 ————— 20 ————[250R]————— 21 ————— 22 ————[250R]—————	 Yellow Orange	19 ————— 20 ————— 21 ————— 22 —————	 Yellow Green



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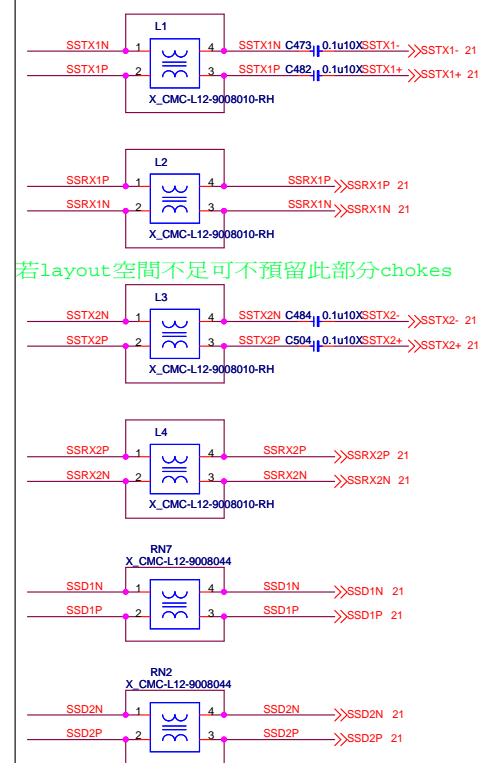
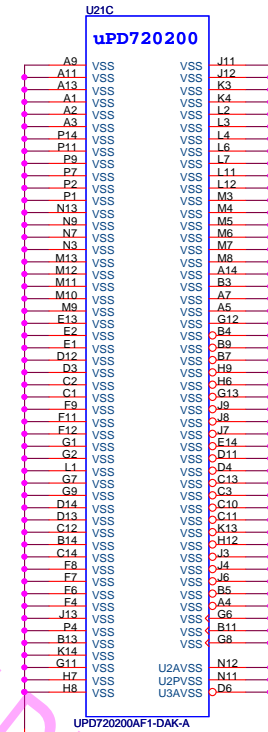
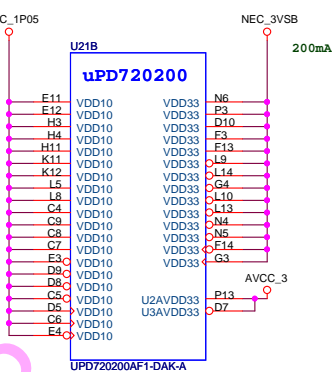
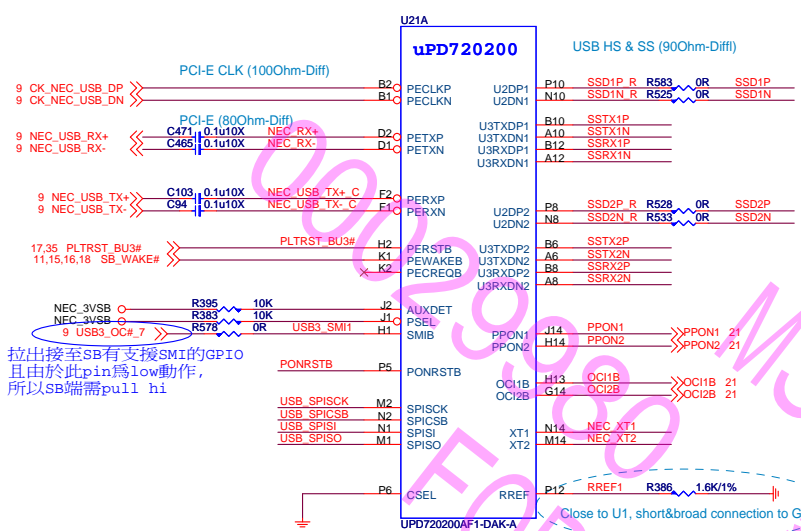
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ALC892
ALC887-VD

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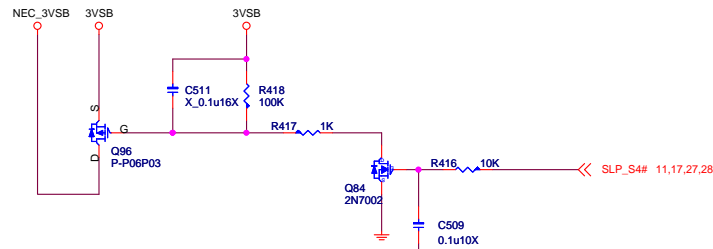
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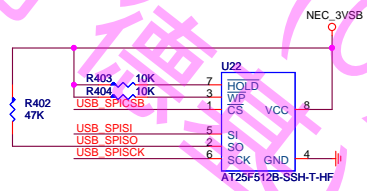


若layout空間不足可不預留此部分chokes

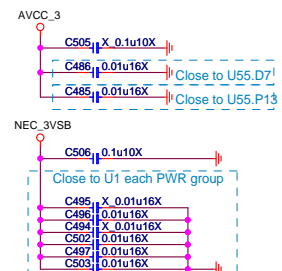
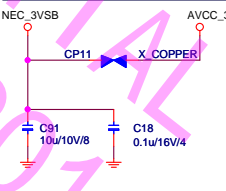
3V_Dual Circuit



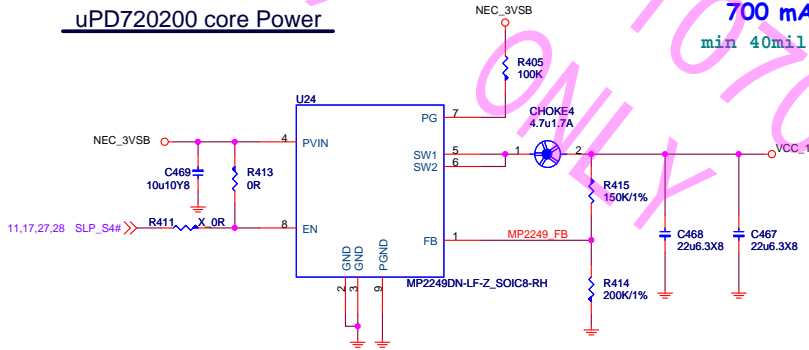
EEPROM



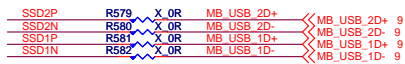
AVCC3 STB Power



uPD720200 core Power

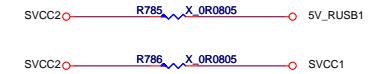
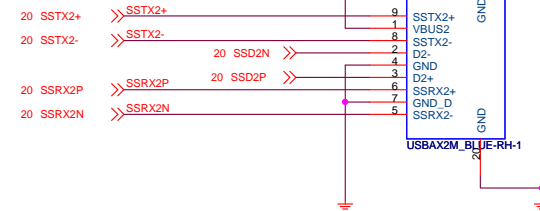
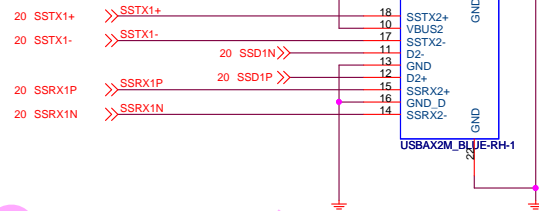


CO-LAY PCH USB2.0



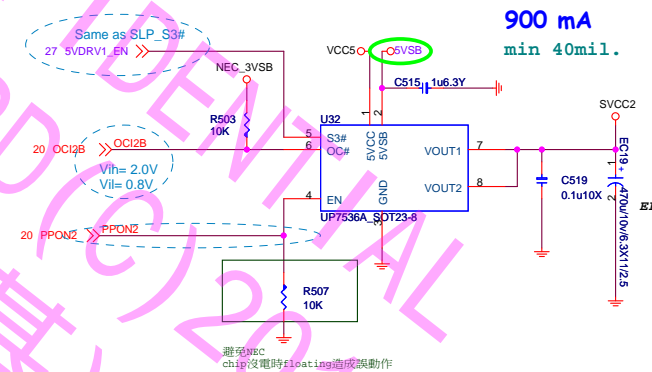
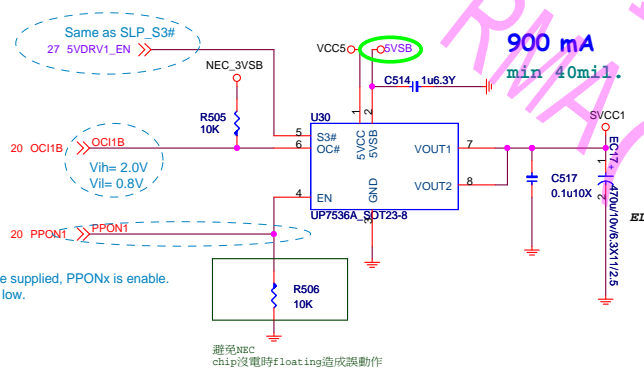
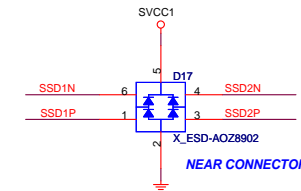
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Rear I/O



ESD Protection

Close to Connector



All power sources of uPD720200 are supplied, PPONx is enable.
PPONx is low when OC1x going to low.

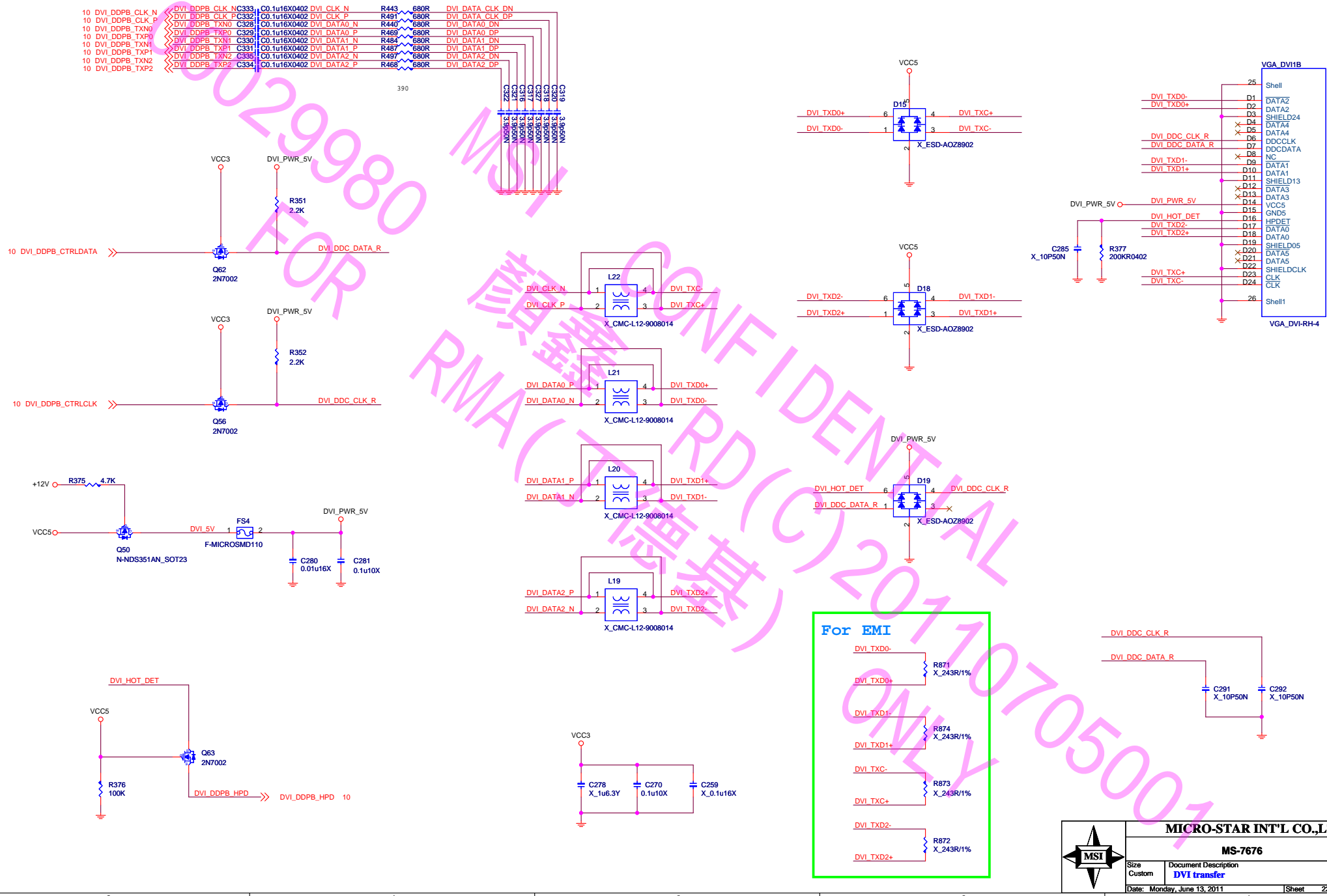
避免nec
chip沒電時floating造成誤動作

避免nec
chip沒電時floating造成誤動作

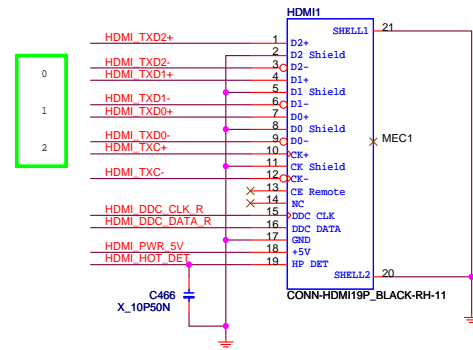
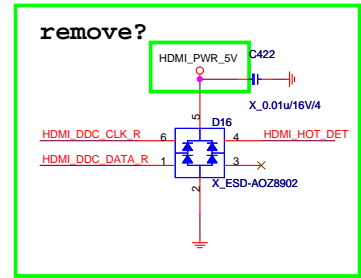
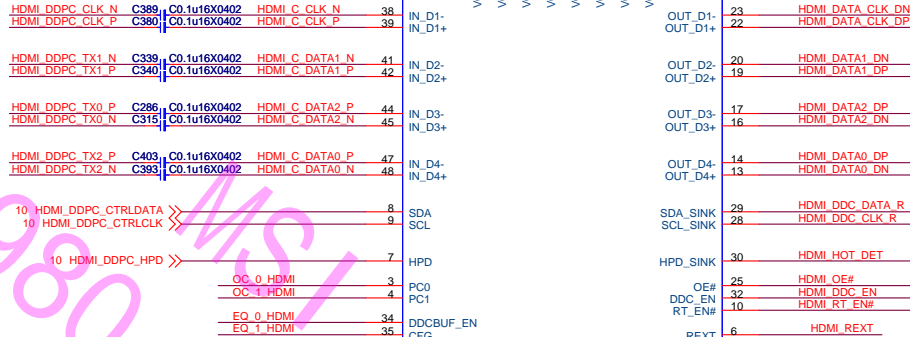
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DVI level shifter

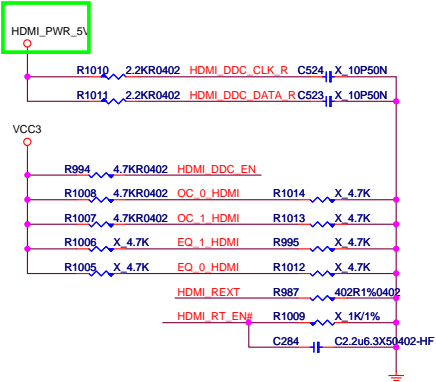
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



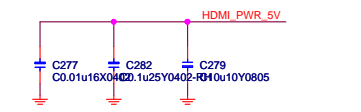
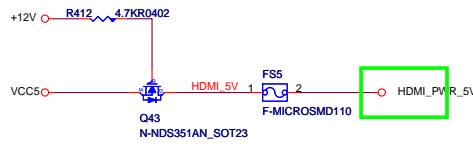
HDMI level shifter



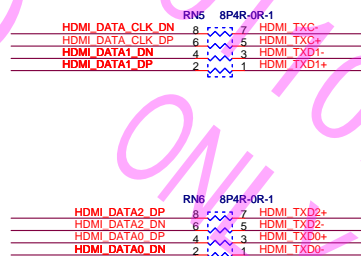
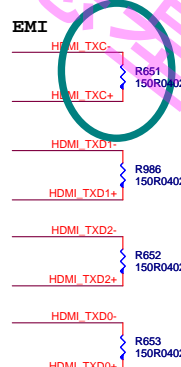
PERICOM料號: B0B-411LS2C-P22.
PARADE料號: B0B-081010C-P97.



注意High/Low Detect




	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.



[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



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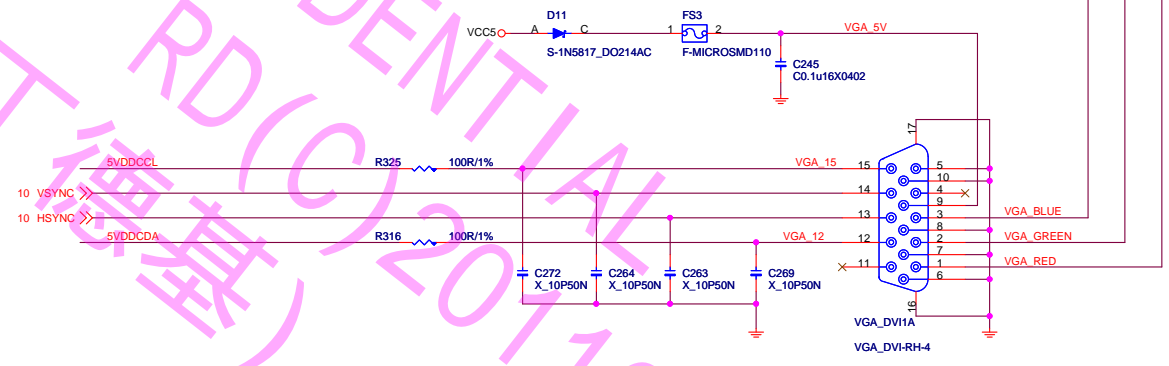
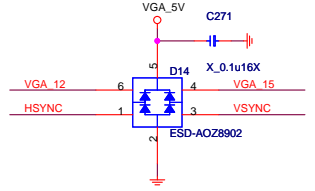
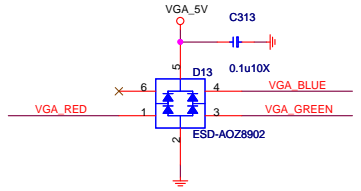
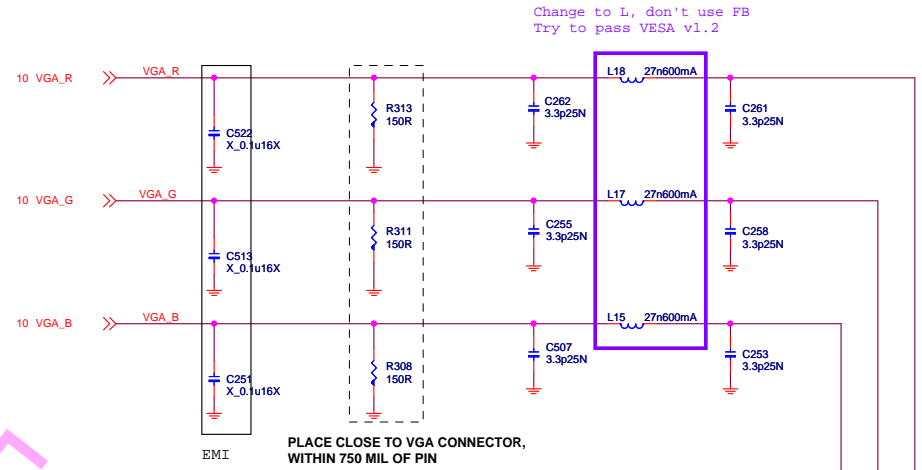
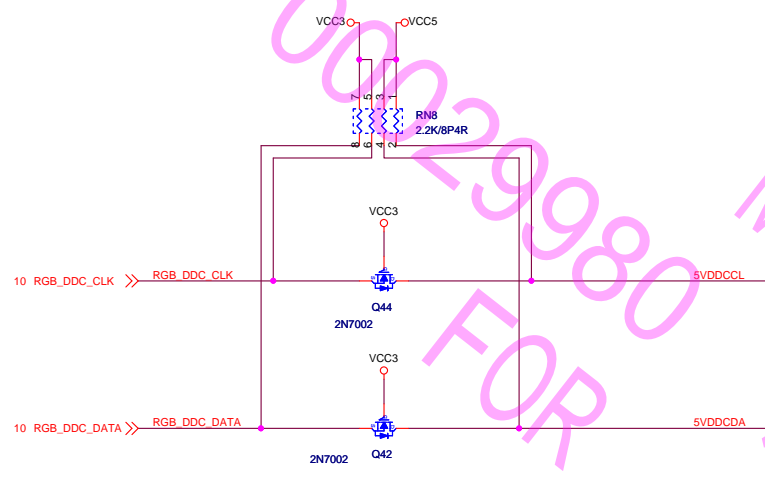
MS-7676


Size Custom	Document Description HDMI	Rev 4.0
Date: Monday, June 13, 2011	Sheet 23 of 39	

D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift



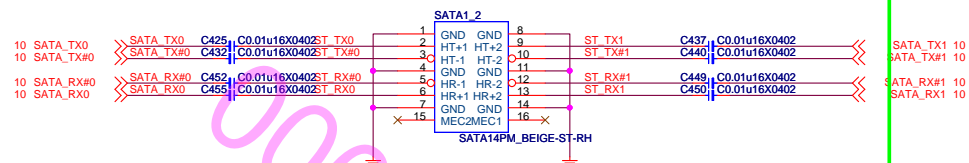


MICRO-STAR INT'L CO.,LTD		
MS-7676		
Size	Document Description	Rev
Custom	VGA	4.0
Date: Monday, June 13, 2011		Sheet 24 of 39

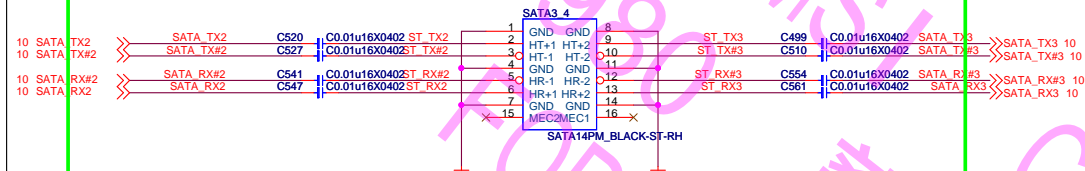
SATA 6G PORT 0,1

H61 PORT 0/1 Support 3G

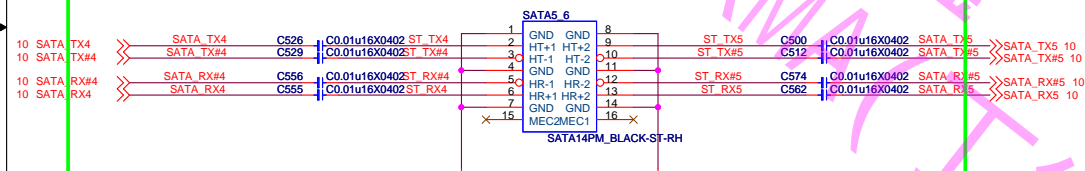
H67 PORT 0/1 Support 6G



SATA 3G PORT 2,3

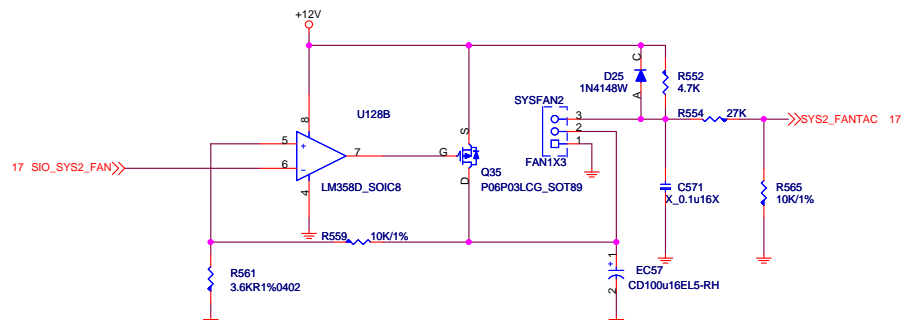


SATA 3G PORT 4,5

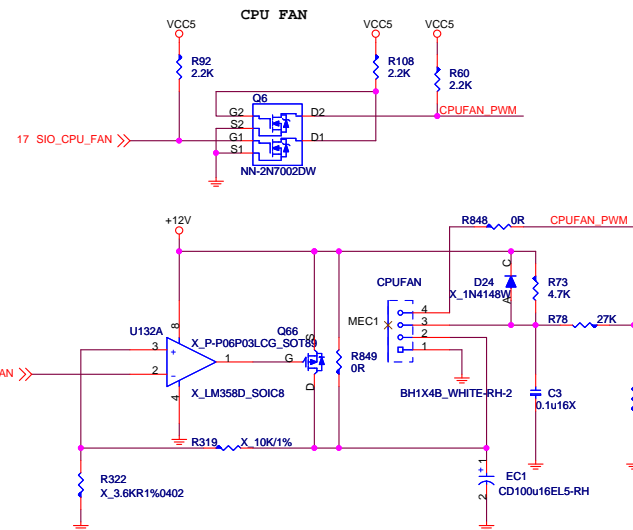


SYSTEM FAN-COUNT CIRCUIT

SYSTEM FAN2

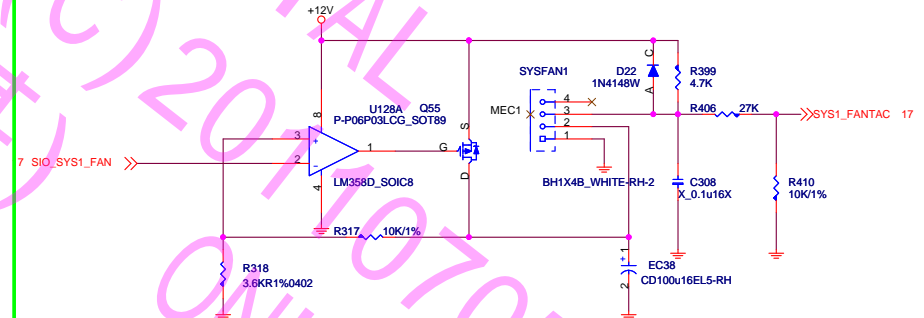


CPU FAN-COUNT CIRCUIT



SYSTEM FAN-COUNT CIRCUIT

SYSTEM FAN1

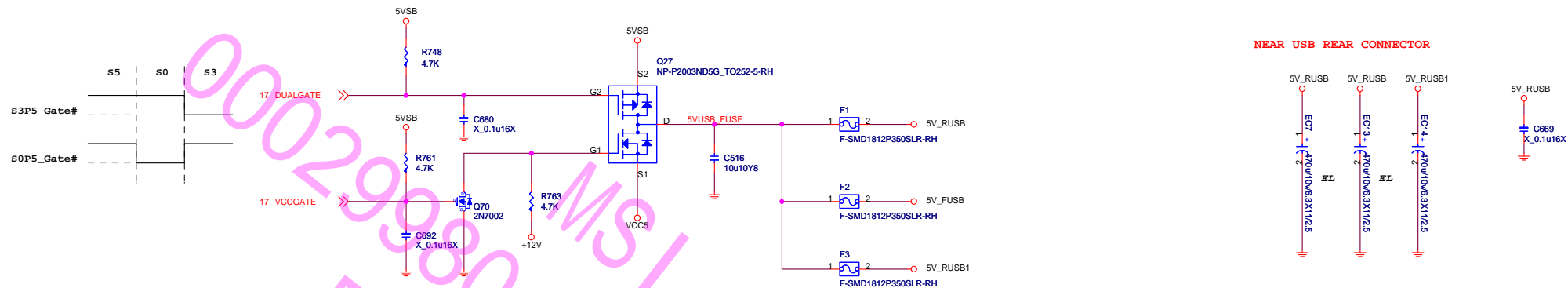


MICRO-STAR INT'L CO.,LTD

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Custom	SATA / FAN Control	4.0
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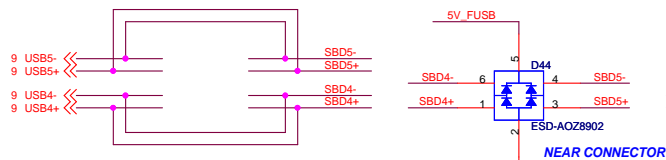
5V_RUSB Switch



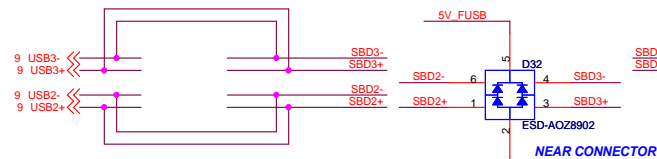
Front USB Connector

For H61 6,7,12,13 Port should be remove

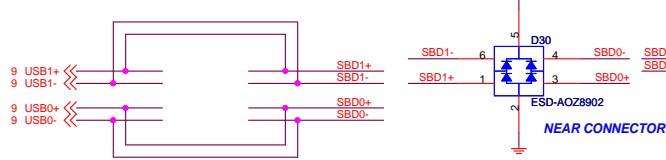
FRONT USB PORT 4,5



FRONT USB PORT 2,3

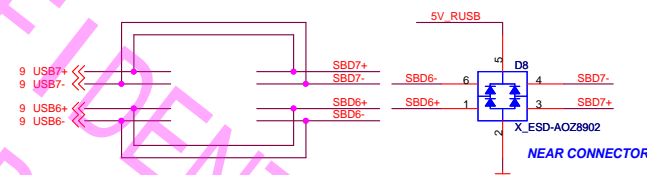


FRONT USB PORT 0,1

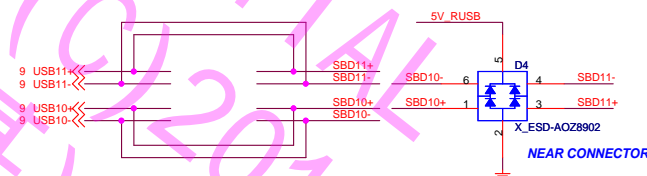


Rear USB Connector

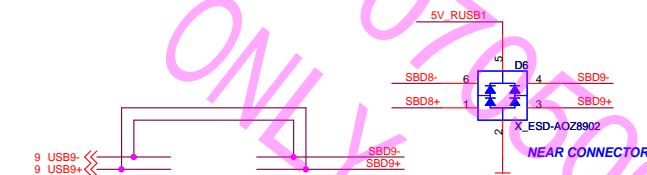
REAR USB PORT 6,7 (With HDMI)



REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9 (With PS2)

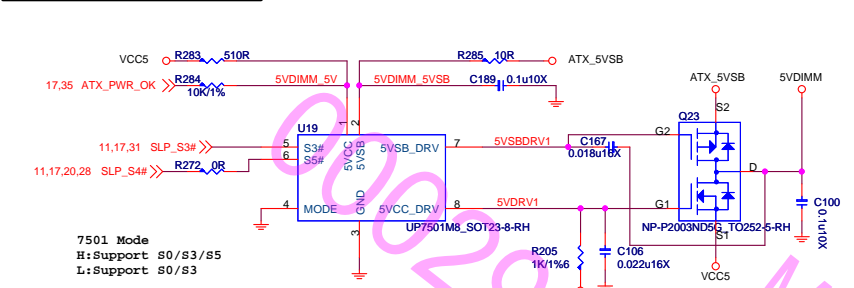


MICRO-STAR INT'L CO.,LTD

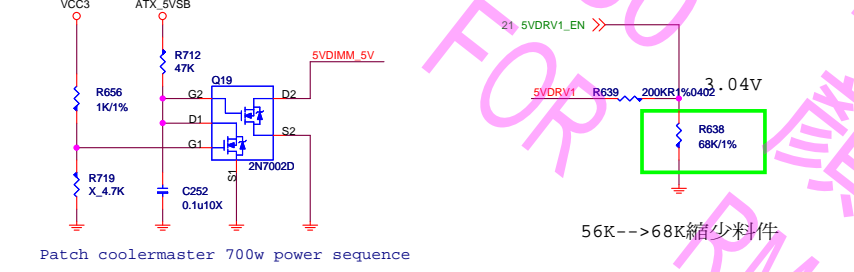
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Custom	USB Connector	4.0
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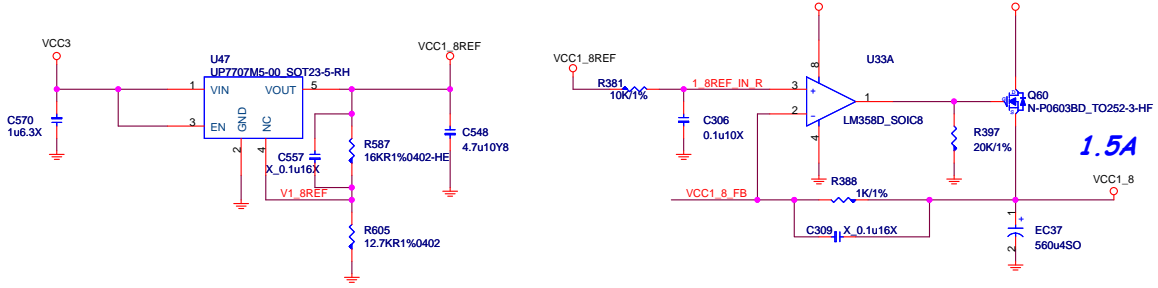
5VDIMM FOR DDR



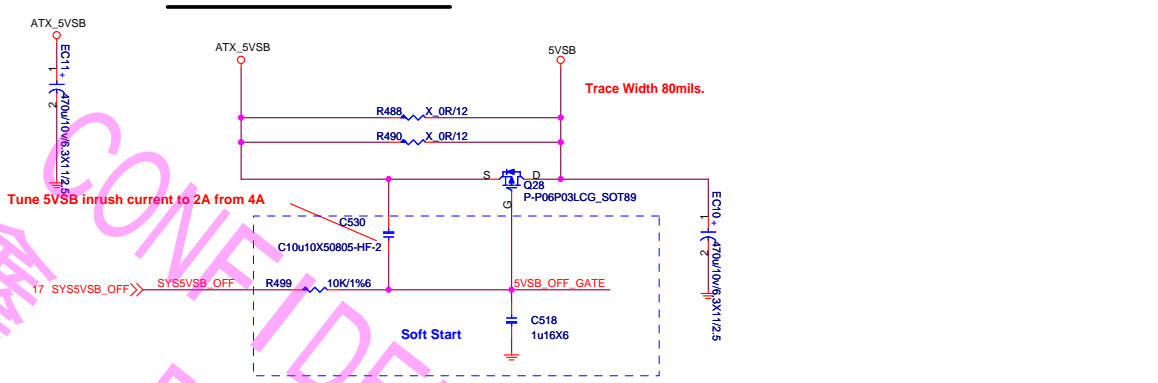
USB MODE



VCC1_8REF

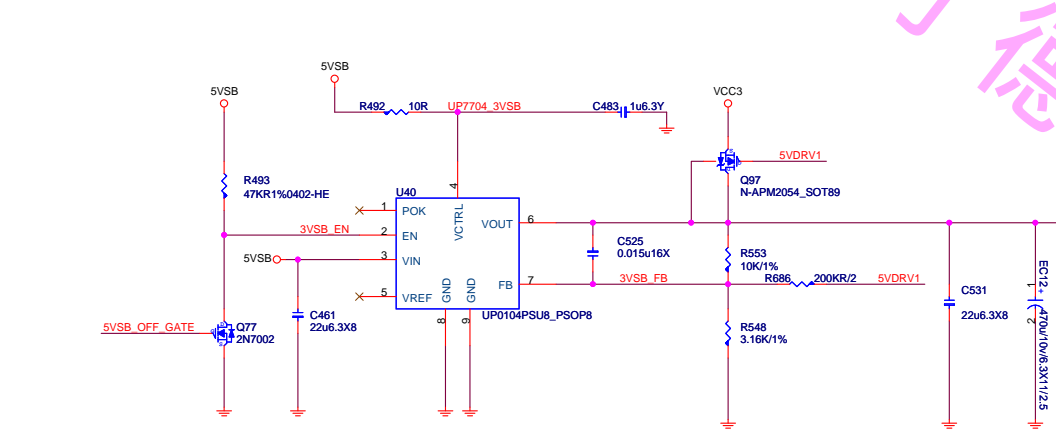


5VSB Power Switch



3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



UPI VOLTAGE CONSOLE

0x2A: RL=10K, RH=OPEN

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



MICRO-STAR INT'L CO.,LTD

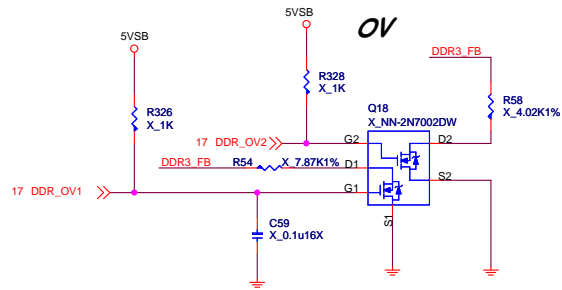
MS-7676

Size Custom Document Description ACPI controller UPI Rev 4.0

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DDR3_1.5V 4.5A+7.5A+1A=13A

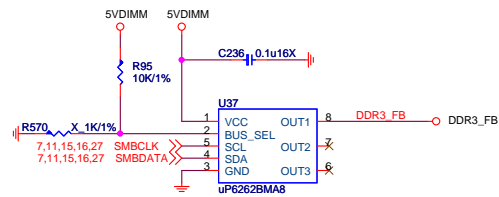
4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT



*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/I/O)
DDR_OV2 = GPIO02(S/I/O)

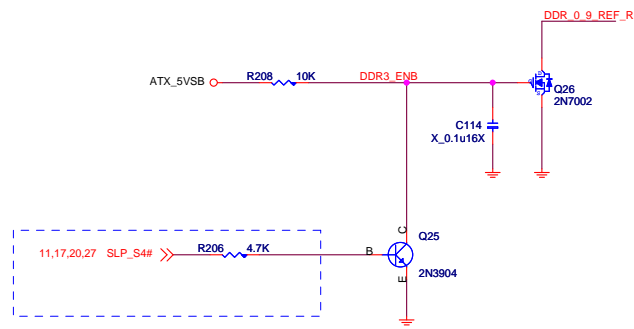


UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

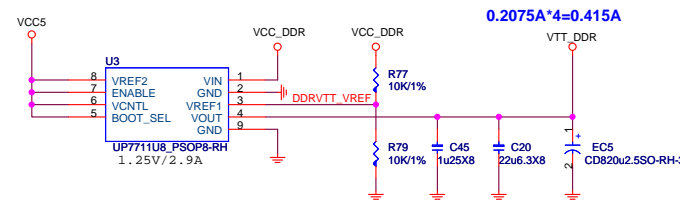
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

P.S. Only for meet Intel power down sequence.



DDR VTT Power

To CPU Copper trace width > 250mils, Fill island behind DIMM > 400mils.

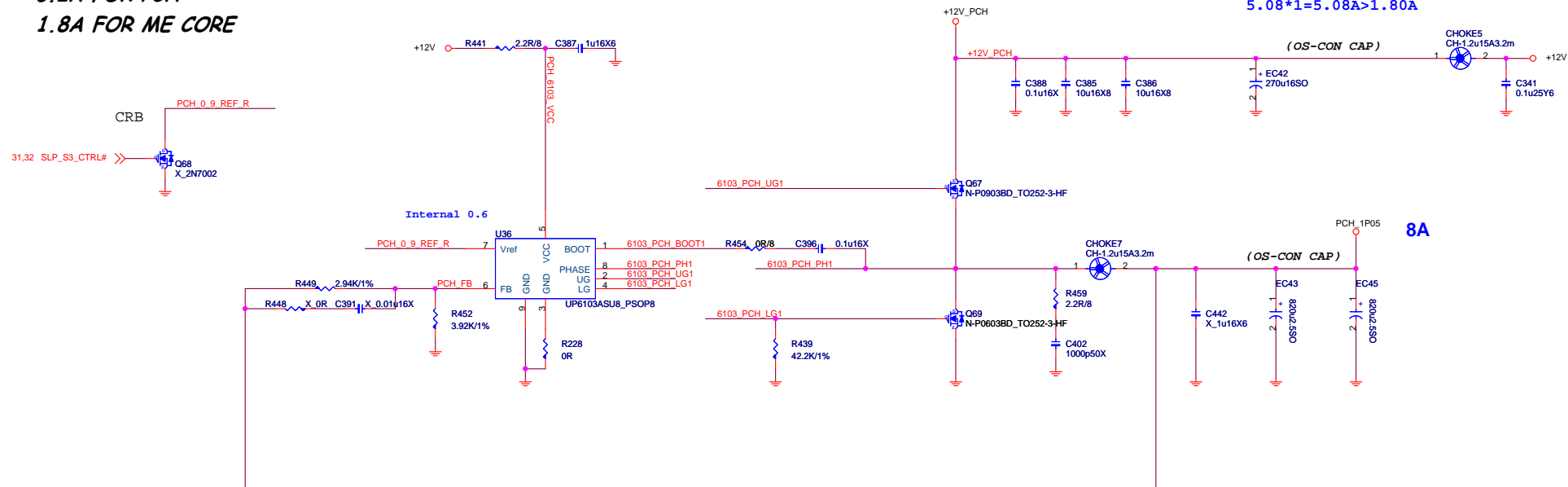


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Size	Document Description	Rev
Custom	DDR Power - uP6103 1-Phase	4.0
Date: Monday, June 13, 2011	Sheet 28 of 39	

1.8A FOR ME CORE

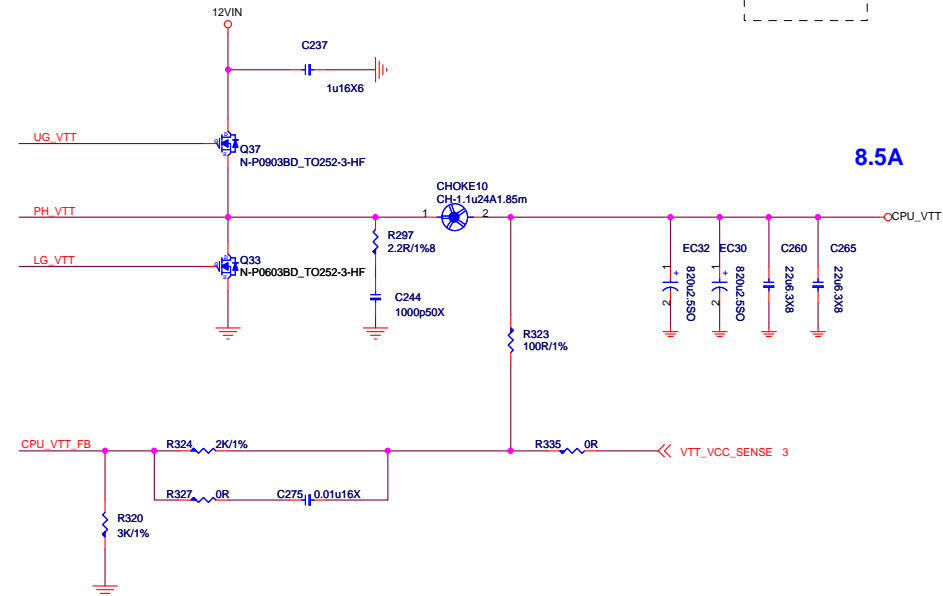
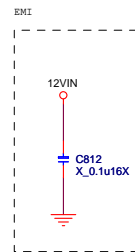
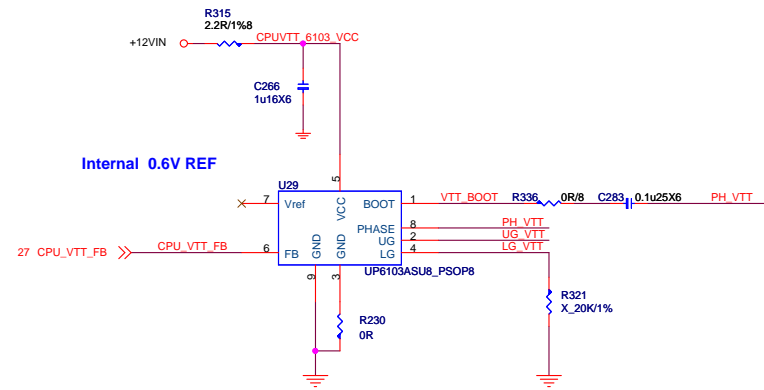
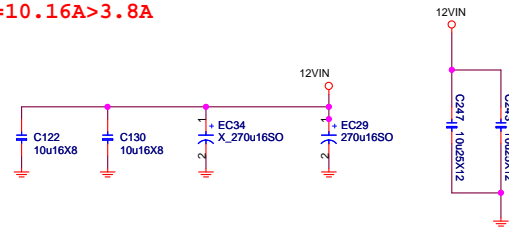


Size Custom	Document Description PCH Power - uP6103 1-Phase	Rev 4.0
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CPU_VTT:1.05/1.00

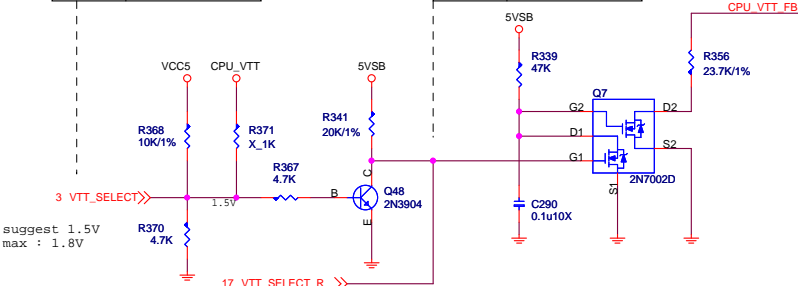
$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$


$I_{ripple} = 1.92(v_{tt}) + 1.88(sa)$
 $5.08 \times 2 = 10.16A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V

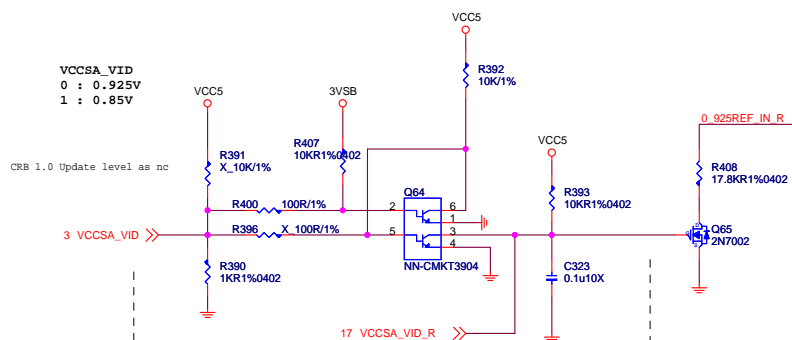
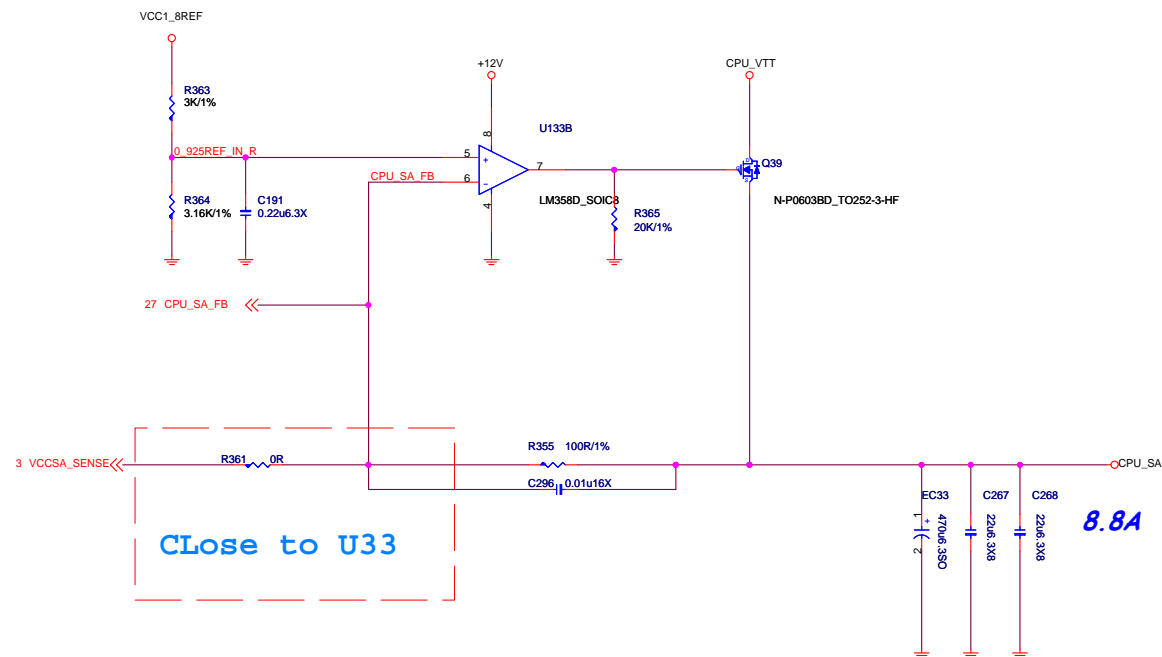
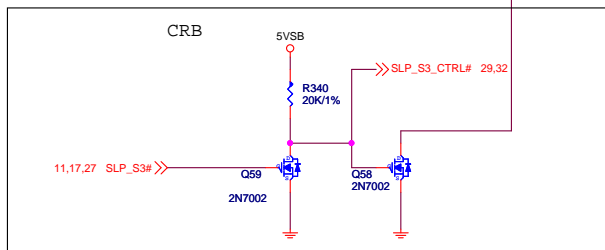
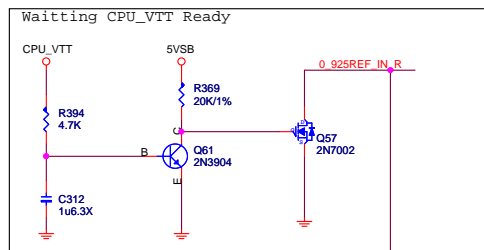




MICRO-STAR INT'L CO.,LTD			
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Size	Document Description	Rev	
Custom	CPU_VTT - uP6103- 1-Phase	4.0	
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CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V

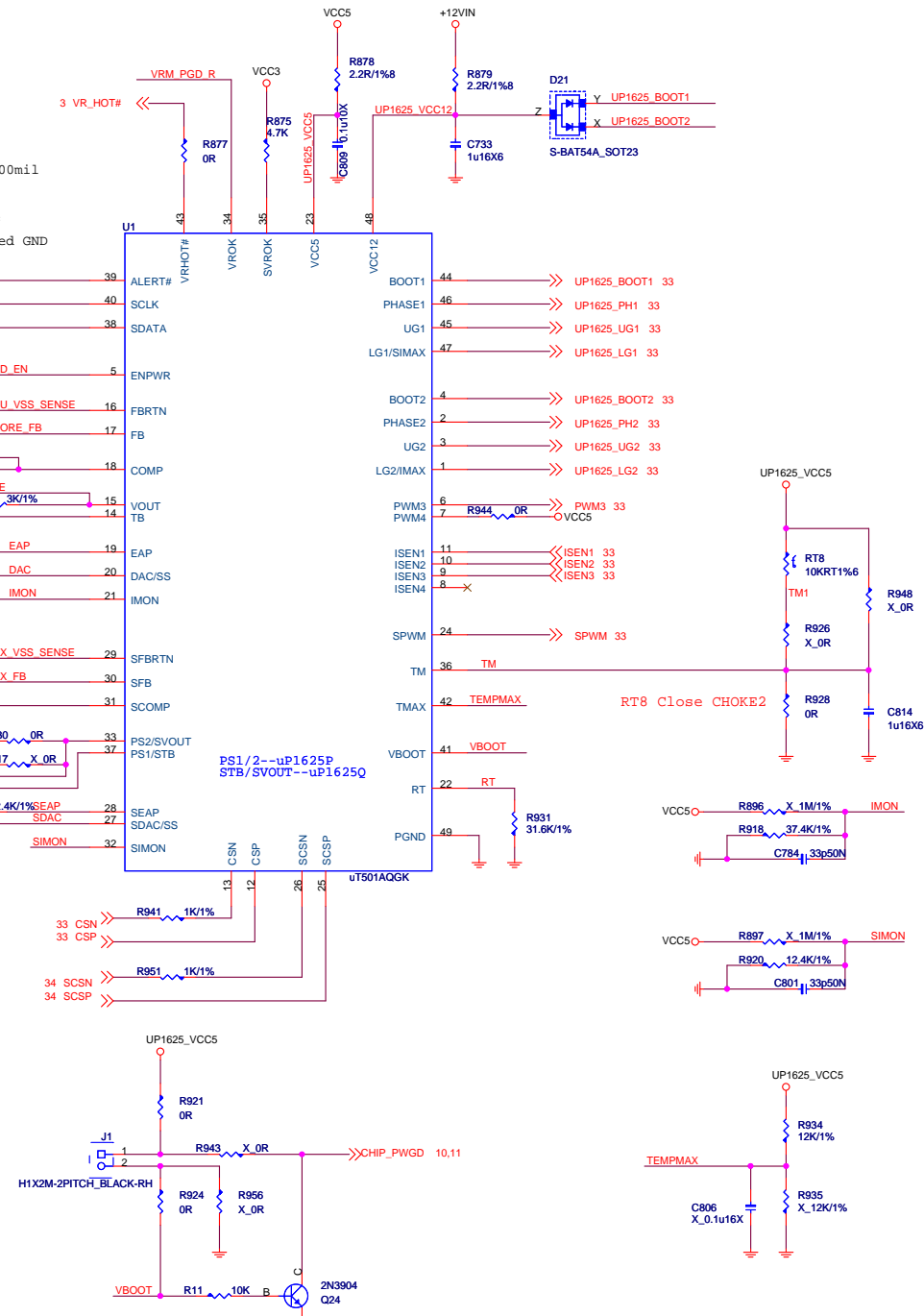
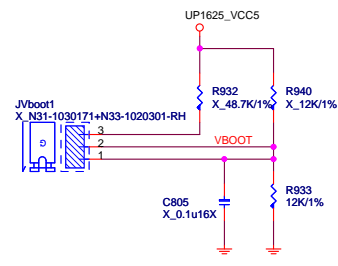
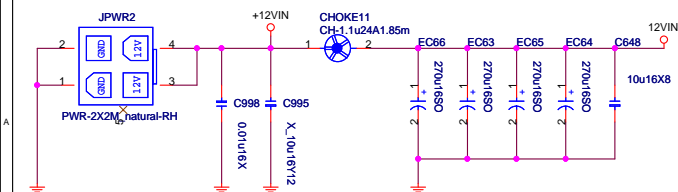
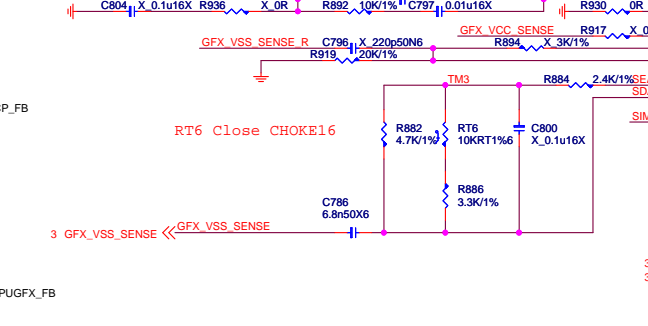
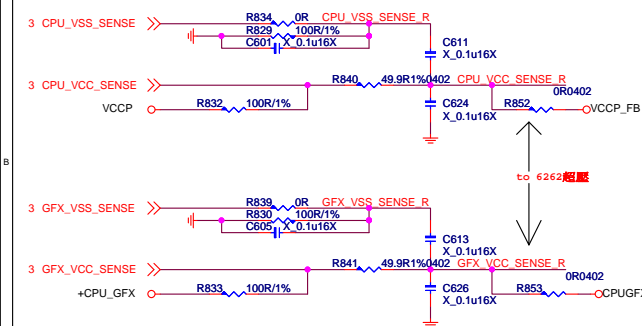
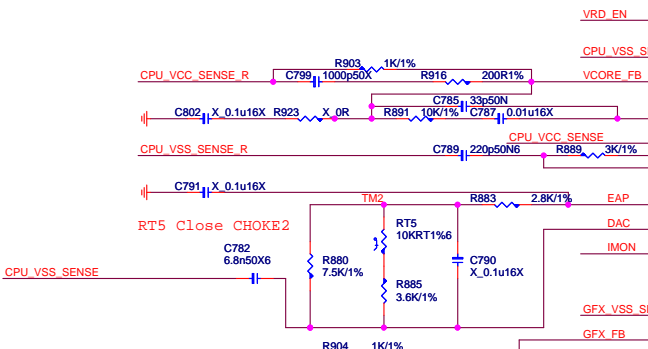
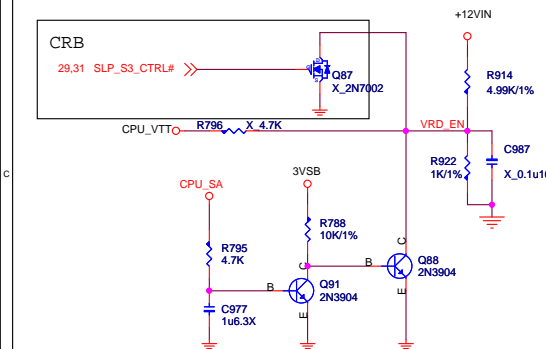
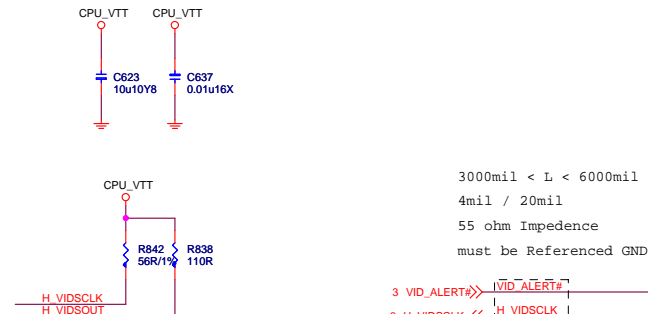
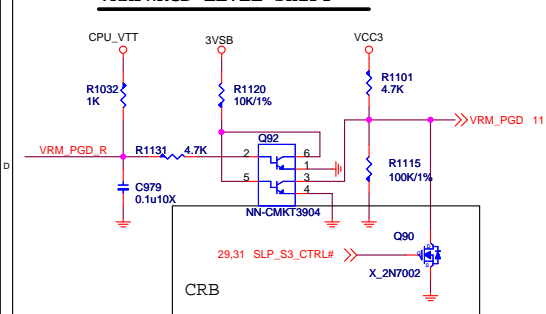


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Custom	CPU_SA - uP6103 1-Phase	4.0
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VRMPWRGD LEVEL SHIFT



Use PWM IC I32-UT5010C-U33(old) --> stuff JVboot1/R932/R933/J1/R943/R956

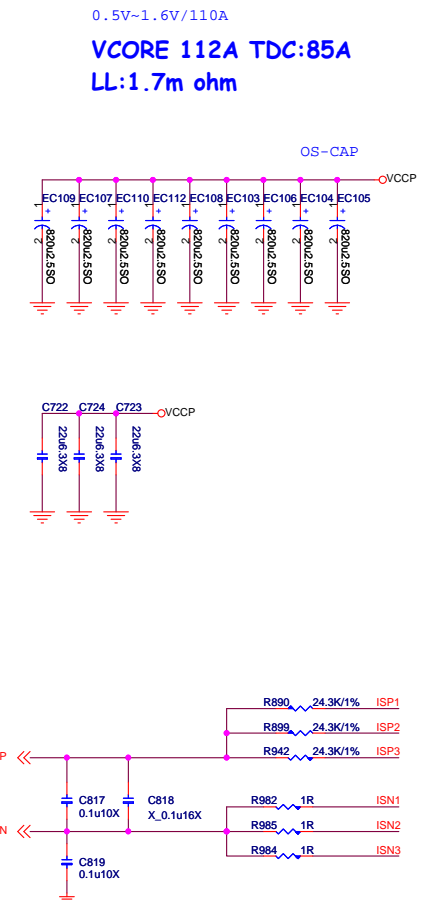
Use PWM IC I32-UT5011C-U33(new) --> stuff J1/R933/R921/R924/R11/Q24



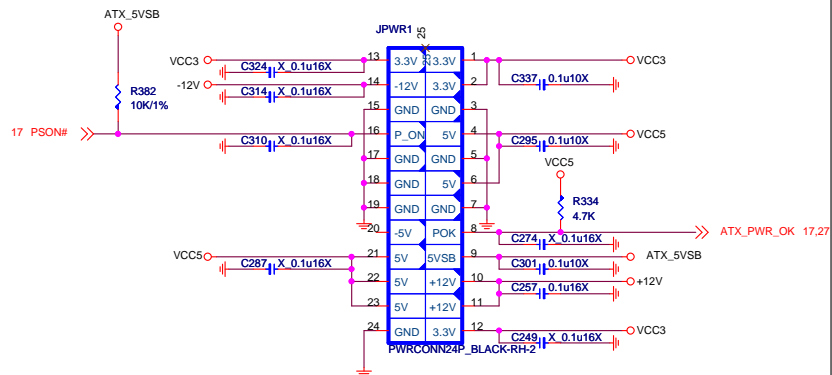
MICRO-STAR INT'L CO.,LTD

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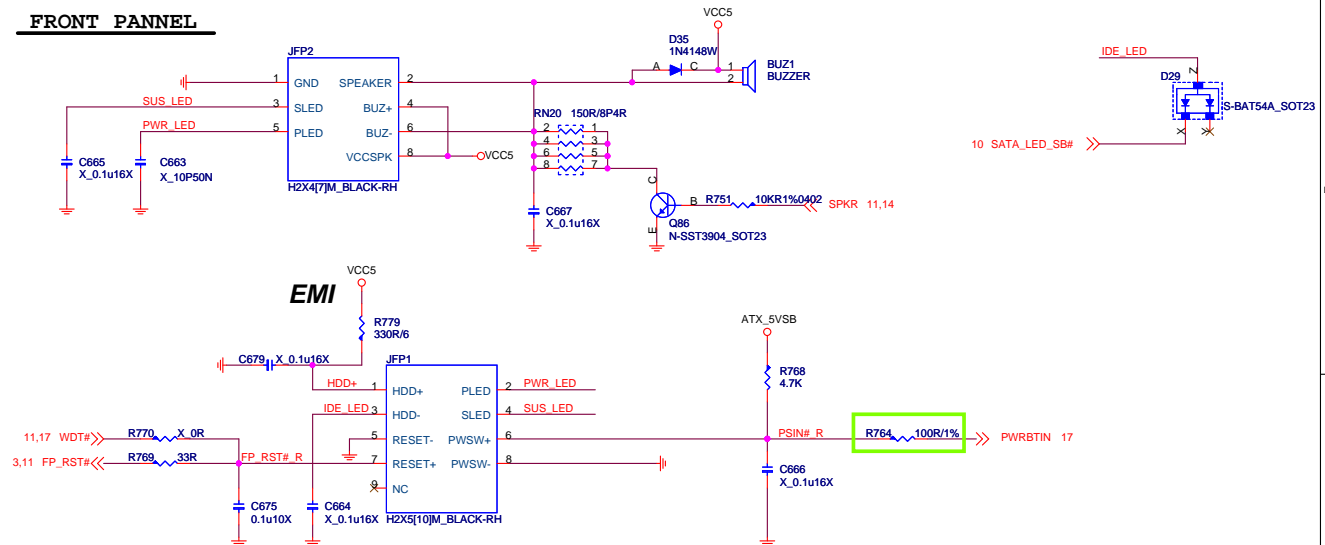
Size Custom	Document Description VRD12 - UT501 3+1-Phase	Rev 4.0
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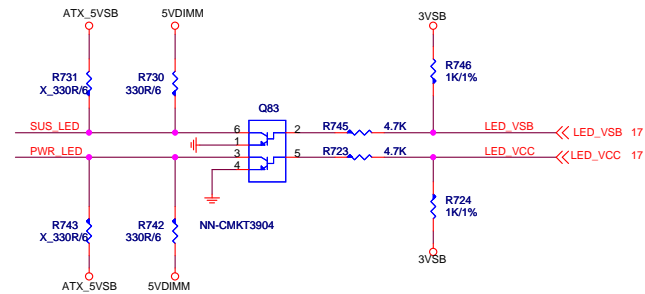
ATX POWER CONNECTOR



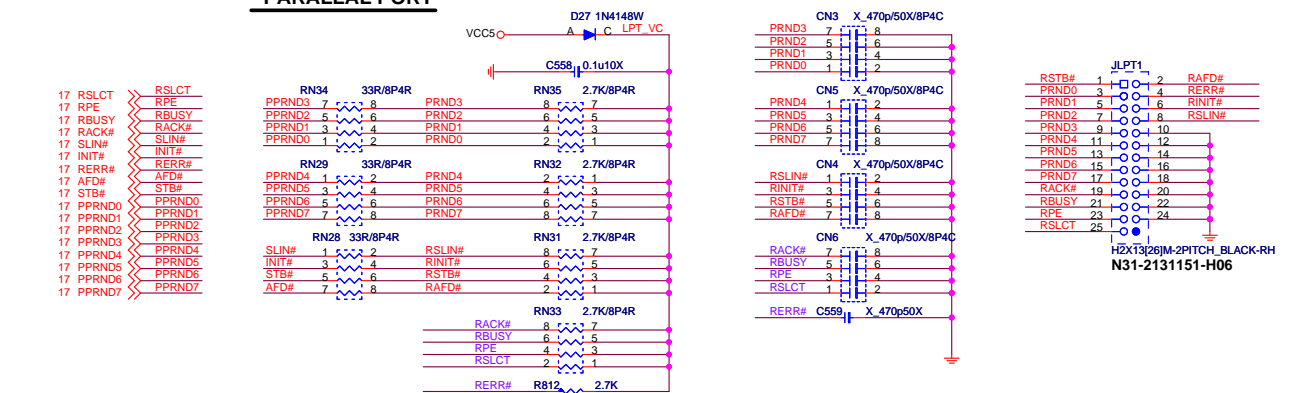
FRONT PANNEL



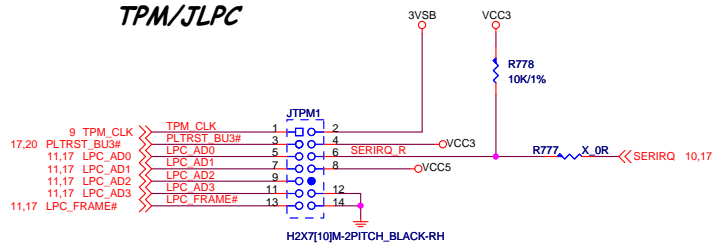
LED (for Fintek 71869)



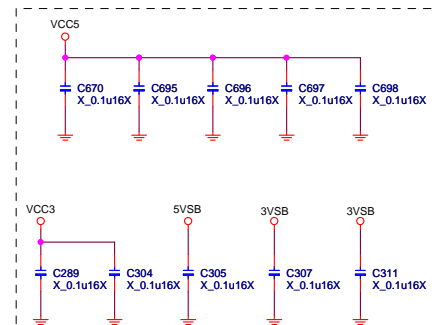
PARALLAL PORT



TPM/JLPC



EMI



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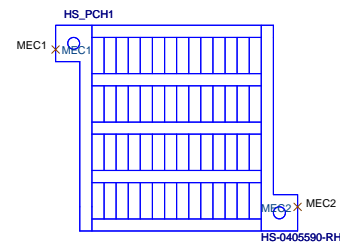
MS-7676-4.0

OPT	Configure	BOM	Function
	H61MU-S01(B3)	601-7680-120	MS-7680 40 H61MU-S01(B3),H61+2DDR3+1*PCI_Ex16+3*PCI_Ex1+4*SATAII+HD 8CH Audio+10USB2.0+2USB3.0+Gb LAN, (EuP),RoHS
A	H61MU-E34(B3)	601-7680-11S	MS-7680 40 OPT:A H61M-E34(B3) Intel H61+2*DDRIII+1*PCIe16,2*PCIe1,1*PCI+DVI/D-sub/HDMI+4*SATAII+10*USB2+HD8Ch Audio+Gb lan,EuP, (All Solid Cap),RoHS

SB

REF10
OPT
X_H67

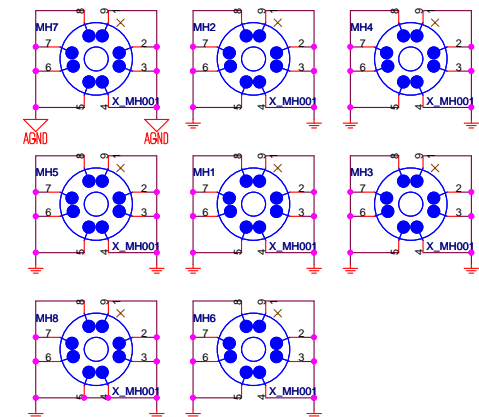
AUDIO CON OPT.

AUDIO10
AUDIO
X_PK/GR/BU/GY/OR/BLPCH XDP PWRGD/RESET

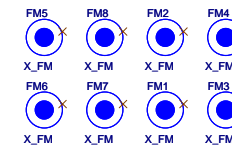
Simulation



Mounting Holes



Optical Fiducial Marks-120



7676-3.0

PK0-0768040-E36, E&E, 23, 寶安恩斯通廠 (MSIS), 4, Coffee
PK0-0768040-E36, E&E, 27, 寶安恩斯通廠 (MSIS), 4, Coffee
PK0-0768040-G37, 精成, 23, 寶安恩斯通廠 (MSIS), 4, Coffee
PK0-0768040-G37, 精成, 27, 寶安恩斯通廠 (MSIS), 4, Coffee

BAT1_X1



BAT-BCR2032P-RH

RUB1



Rubber

RUB2



Rubber

CPU_H1



E21-7557050-L06

HDMI_LA1



HDMI LABEL

THX1



THX LABEL

VIRTU_LA1



VIRTU LABEL



MICRO-STAR INT'L CO.,LTD

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